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IH11K-MHS

H110MG PRO

VER 6.1

CPU:
Intel Skylake S 42 in LGA1151 Package 95W

System Chipset:
SPT-H PCH

Main Memory:
Dual Channel/DDR-III*2(Max 16GB) 1066/1333/1600

Onboard Device:
Super I/O:IT8613E
LAN:Realtek 8111H
HD Codec:ALC887


Power solution:
CPU Voltage Regulators:3phase by RT3606 high 1 Low 1 OV by RT3606
DDR Voltage Regulators:1Phase by UP1514 high 1 Low 1 OV by IT8613E

Expansion Slots:
PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT *2

REAR IO:
PS/2 PORT
DVI Port
VGA Port
USB3.0 PORT *2
Gb RJ-45 +2 layer USB3.0 Ports
Audio Jackets (3 PORT)

Front I/O:
SATA3 *6
USB 2.0 Header * 2 Serial header
USB 3.0 Header * 1 Front Audio Header
CPU FAN *1
System FAN *1

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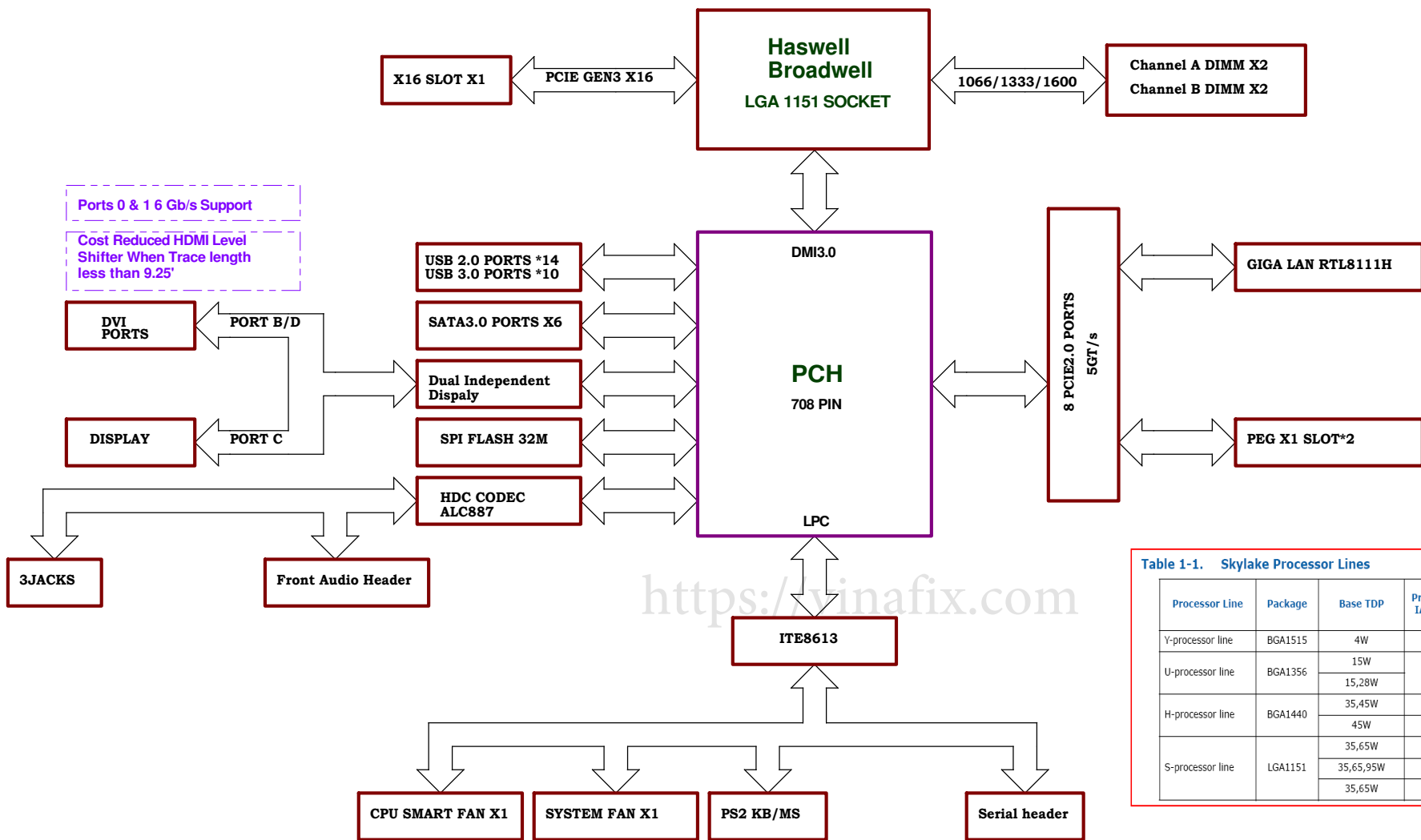
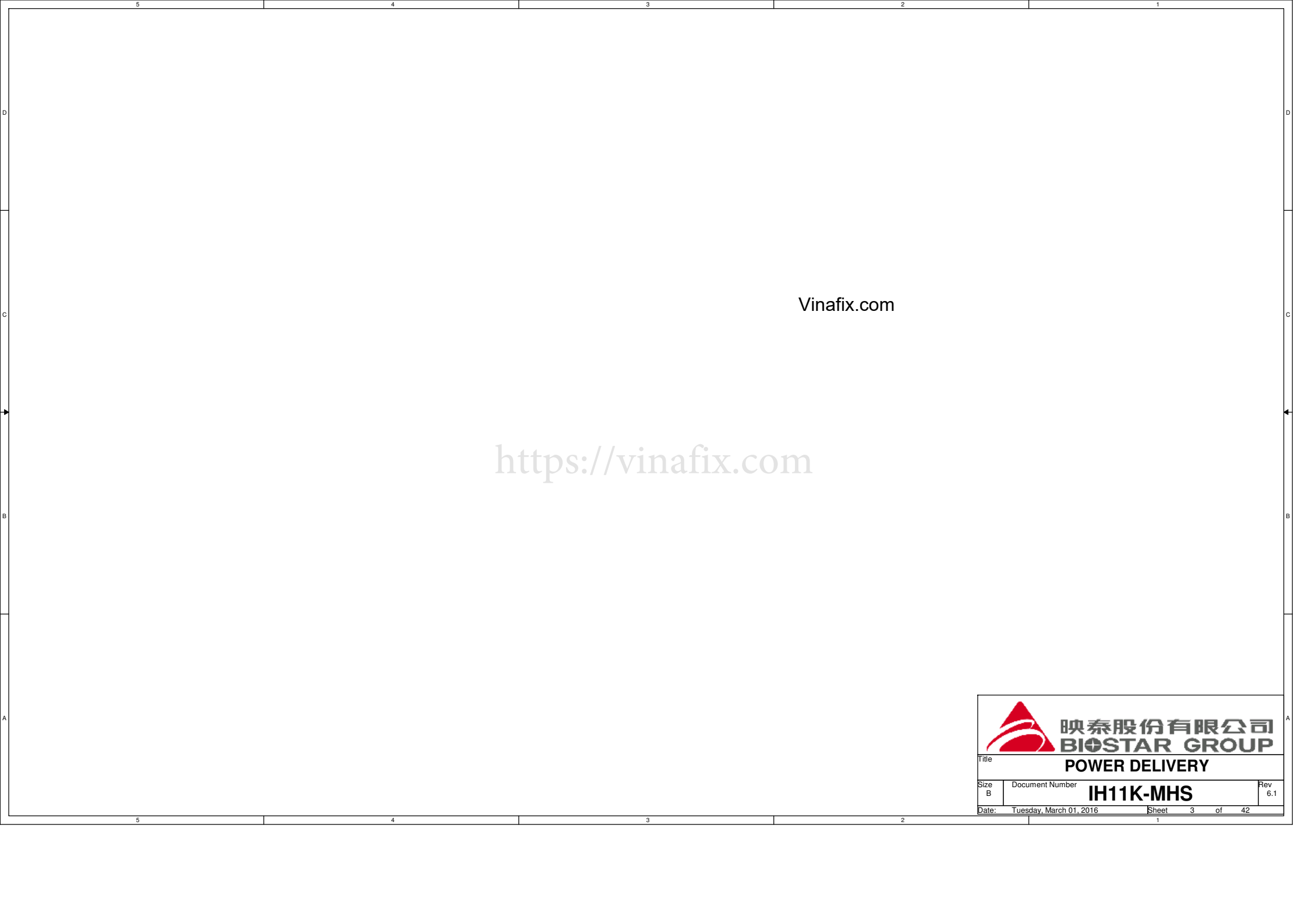



Table 1-1. Skylake Processor Lines						
Processor Line	Package	Base TDP	Processor IA Cores	Maximum Graphics Configuration	On Package Cache	Platform Type
Y-processor line	BGA1515	4W	2	GT2	N/A	1-Chip
U-processor line	BGA1356	15W	2	GT2	64 MB	1-Chip
		15,28W		GT3		
H-processor line	BGA1440	35,45W	4	GT2	N/A	2-Chip
		45W	4	GT4	128 MB	
S-processor line	LGA1151	35,65W	2	GT2	N/A	2-Chip
		35,65,95W	4	GT2		
		35,65W	4	GT4	64 MB	



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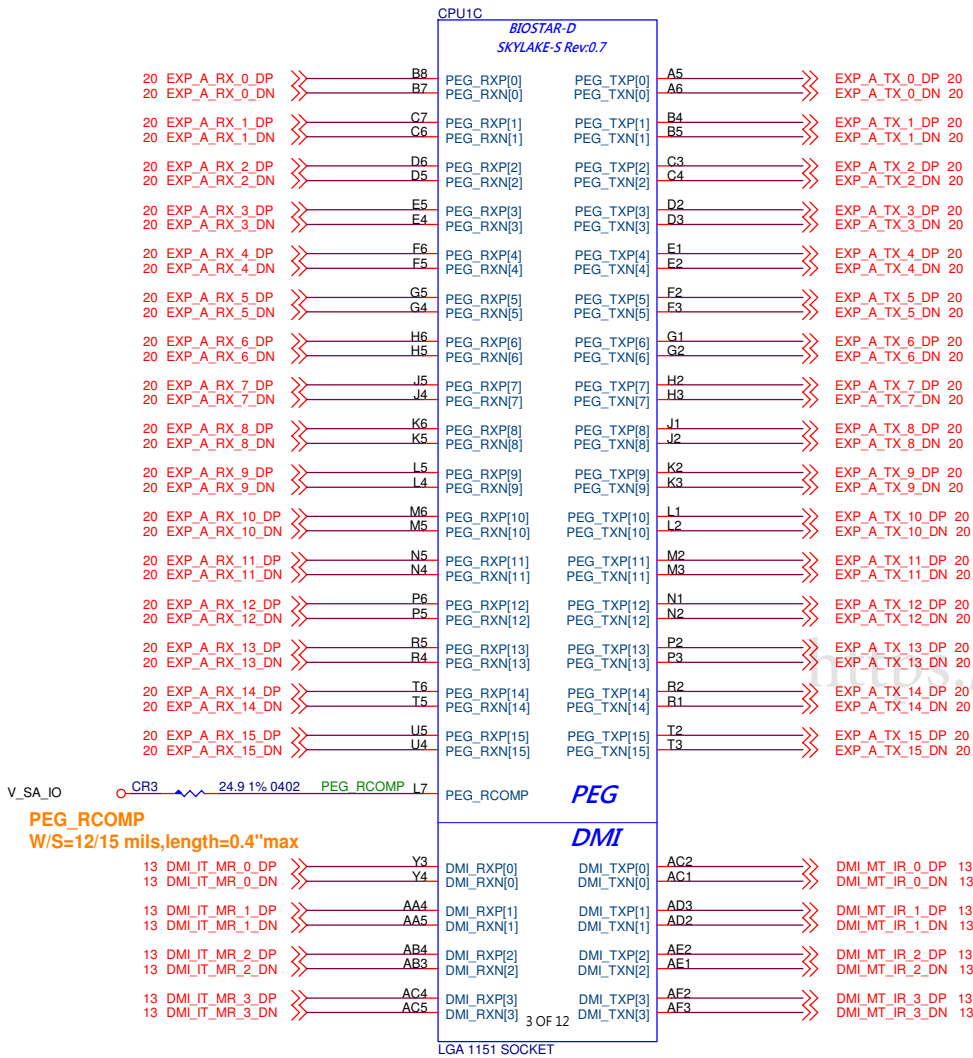
1.VER0.60:REMOVE SATA EXPRESS CONN(PAGE14/16/17/24)
2.VER0.60:REMOVE Hi-Fi FUNCTION(PAGE23/28/29)
3.VER0.60:CHANGE CPU POWER CONN TO 2*2(PAGE39)
4.VER0.60:NEW ADD COLAY FOR V_SA_IO(PAGE38)
5.VER0.6:COST DOWN(POWER_JUSB1 COLAY POWER_JUSB2)(PAGE26)
6.VER0.6:COST DOWN(REMOVE CT6)(PAGE26)
7.VER0.6:COST DOWN(MODIFY F6/GF3 SIZE)(PAGE21/34)
8.VER0.6:COST DOWN(MODIFY MC36 SIZE)(PAGE11)
9.VER0.6:COST DOWN(MCT2/3/CT11 CHANGE TO 560UF)(PAGE31/32)
10.VER0.6:COST DOWN(MC38 /NI)(PAGE11)
11.VER0.6:COST DOWN(YC23 /NI)(PAGE18)
12.VER0.6:COST DOWN(YC16/17/21 /NI)(PAGE18)
13.VER0.6:COST DOWN(LC18/MC5/6 CHANGE TO 10UF 0603 SIZE)(PAGE11/27)
14.VER0.6:COST DOWN(PCI55 CHANGE TO 10UF 0603 SIZE)(PAGE39)
15.VER0.6:COST DOWN(C165/MC9 CHANGE TO 1UF 0805 SIZE)(PAGE31/38)
16.VER0.6:COST DOWN(YC11/26 /NI)(PAGE18)
17.VER0.6:COST DOWN(CHANGE TO RN 8P4R)(PAGE17)
18.VER0.6:ATXPG MODIFY(PAGE23/36)
19.VER0.6:COST DOWN(PAGE33)
20.VER0.6:COST DOWN(2N7002 CHANGE TO 2N3904)(PAGE30/33/39)
21.VER0.6:COST DOWN(SHORT 0402)(PAGE8/11/12/16/19/23/33/39)
22.VER0.6:COST DOWN(SHORT 0805)(PAGE18/37/39/40)
23.VER0.6:COST DOWN(BEAD COLAY)(PAGE29)
24.VER0.6:COST DOWN(CPU PWM CHANHE TO RT3606)(PAGE39/40/41)
25.VER0.6:COST DOWN(POWER_JUSB4/POWER_JUSB5 COLAY)(PAGE25/34)
26.VER0.6:MIC MODIFY BY KEVIN(PAGE28)
27.VER0.6:ACPI MODIFY BY KEVIN(PAGE30)
28.VER0.6:IO MODIFY BY KEVIN(PAGE23/27)
29.VER0.6:V_SA_IO MODIFY BY KEVIN(PAGE38)
30.VER0.65:PCIECLKRQ2# MODIFY(PAGE17)

31.VER0.65:PU1 core power change to +12V(PAGE39)
32.VER0.65:SET2_3606 MODIFY(PAGE39)
33.VER0.65:PWM FAE MODIFY(PAGE40/41)
34.VER0.65:IO MODIFY BY PETER(PAGE23)
35.VER0.65:DDR4_DRAMRST_N MODIFY BY PETER(PAGE11)
36.VER0.65:NEW ADD SATA CONN(PAGE14/24)
37.VER0.65:NEW ADD 100UF COLAY CAP(PAGE30/31/32)
38.VER6.0:NEW ADD 100UF AUDIO CAP(PAGE28)

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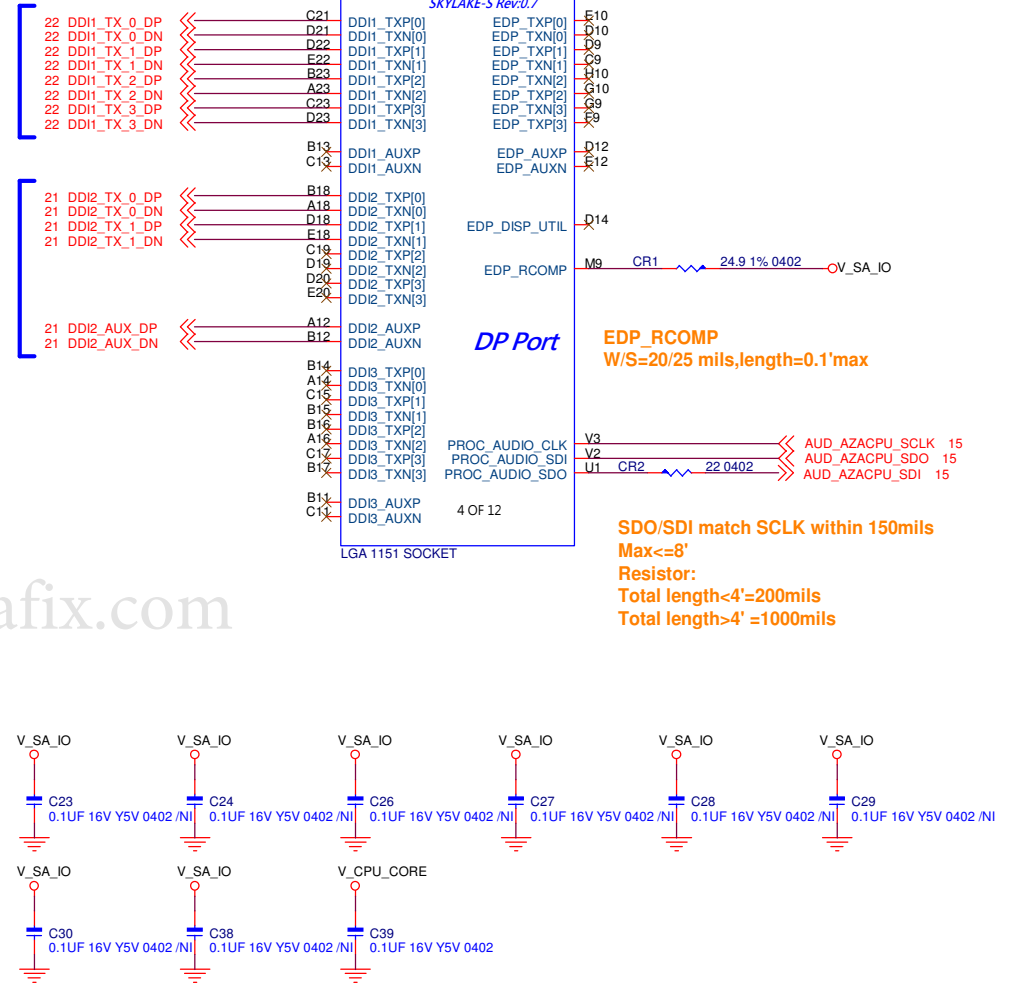
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DVI PORT

EDP to VGA



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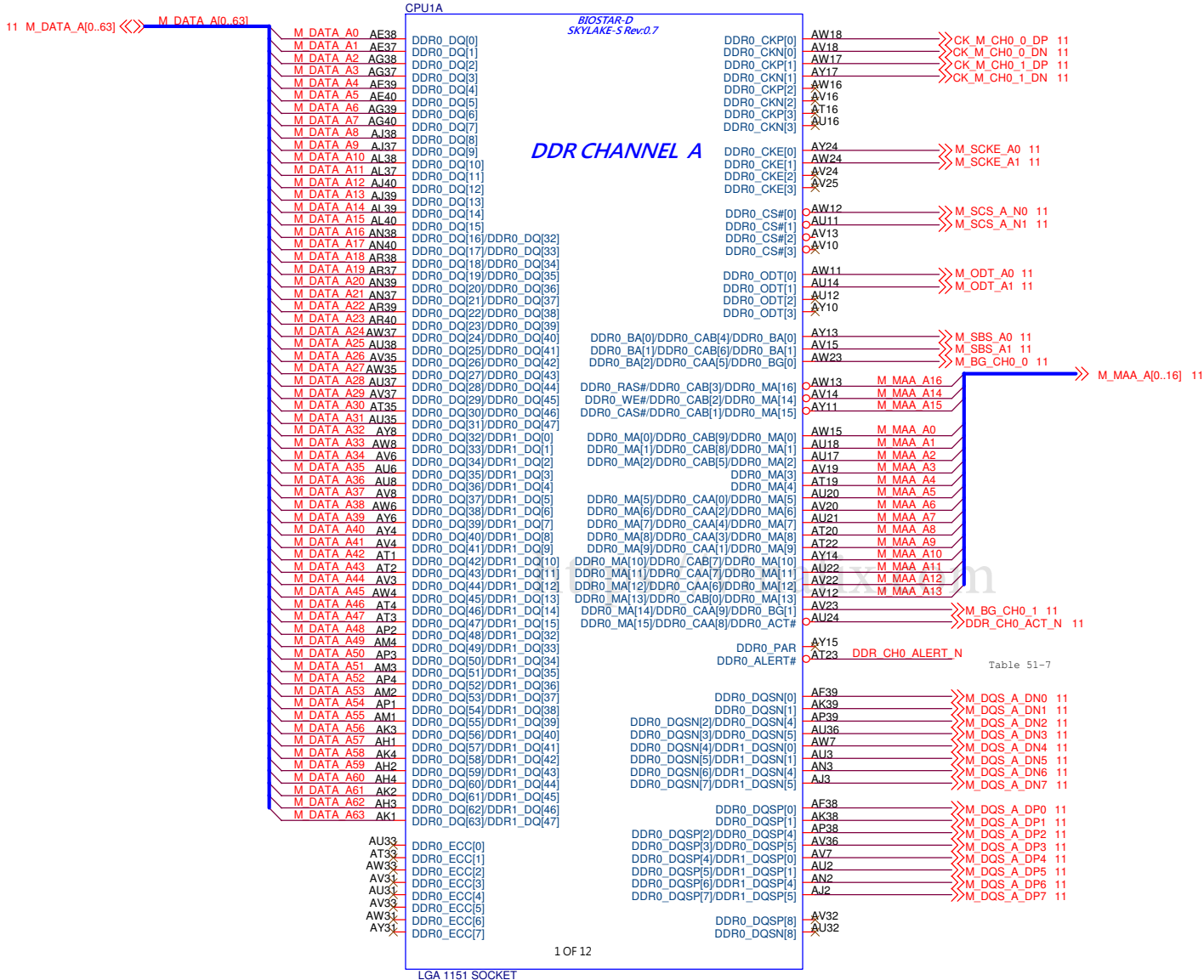
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Title: **CPU PCIEX16/DMI/FDI**

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Title

CPU DDR3 CHANNEL A

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12 M_DATA_B[0..63] <<< M_DATA_B[0..63]

M_DATA_B0 AD34
M_DATA_B1 AD35
M_DATA_B2 AG35
M_DATA_B3 AH35
M_DATA_B4 AE35
M_DATA_B5 AE34
M_DATA_B6 AG34
M_DATA_B7 AH34
M_DATA_B8 AK35
M_DATA_B9 AL35
M_DATA_B10 AK32
M_DATA_B11 AL32
M_DATA_B12 AK34
M_DATA_B13 AL34
M_DATA_B14 AK31
M_DATA_B15 AL31
M_DATA_B16 AP35
M_DATA_B17 AN35
M_DATA_B18 AN32
M_DATA_B19 AP32
M_DATA_B20 AN34
M_DATA_B21 AP34
M_DATA_B22 AN31
M_DATA_B23 AP31
M_DATA_B24 AL29
M_DATA_B25 AM29
M_DATA_B26 AP29
M_DATA_B27 AR29
M_DATA_B28 AM28
M_DATA_B29 AL28
M_DATA_B30 AP28
M_DATA_B31 AP28
M_DATA_B32 AR12
M_DATA_B33 AP12
M_DATA_B34 AM13
M_DATA_B35 AL13
M_DATA_B36 AR13
M_DATA_B37 AP13
M_DATA_B38 AM12
M_DATA_B39 AL12
M_DATA_B40 AP10
M_DATA_B41 AR10
M_DATA_B42 AR7
M_DATA_B43 AP7
M_DATA_B44 AR9
M_DATA_B45 AP9
M_DATA_B46 AR6
M_DATA_B47 AP6
M_DATA_B48 AM10
M_DATA_B49 AL10
M_DATA_B50 AM7
M_DATA_B51 AL7
M_DATA_B52 AM9
M_DATA_B53 AL9
M_DATA_B54 AM6
M_DATA_B55 AL6
M_DATA_B56 AJ6
M_DATA_B57 AJ7
M_DATA_B58 AE6
M_DATA_B59 AE7
M_DATA_B60 AH7
M_DATA_B61 AH6
M_DATA_B62 AE7
M_DATA_B63 AE6

CPU1B

DDR1_DQ[0]/DDR0_DQ[16]
DDR1_DQ[1]/DDR0_DQ[17]
DDR1_DQ[2]/DDR0_DQ[18]
DDR1_DQ[3]/DDR0_DQ[19]
DDR1_DQ[4]/DDR0_DQ[20]
DDR1_DQ[5]/DDR0_DQ[21]
DDR1_DQ[6]/DDR0_DQ[22]
DDR1_DQ[7]/DDR0_DQ[23]
DDR1_DQ[8]/DDR0_DQ[24]
DDR1_DQ[9]/DDR0_DQ[25]
DDR1_DQ[10]/DDR0_DQ[26]
DDR1_DQ[11]/DDR0_DQ[27]
DDR1_DQ[12]/DDR0_DQ[28]
DDR1_DQ[13]/DDR0_DQ[29]
DDR1_DQ[14]/DDR0_DQ[30]
DDR1_DQ[15]/DDR0_DQ[31]
DDR1_DQ[16]/DDR0_DQ[48]
DDR1_DQ[17]/DDR0_DQ[49]
DDR1_DQ[18]/DDR0_DQ[50]
DDR1_DQ[19]/DDR0_DQ[51]
DDR1_DQ[20]/DDR0_DQ[52]
DDR1_DQ[21]/DDR0_DQ[53]
DDR1_DQ[22]/DDR0_DQ[54]
DDR1_DQ[23]/DDR0_DQ[55]
DDR1_DQ[24]/DDR0_DQ[56]
DDR1_DQ[25]/DDR0_DQ[57]
DDR1_DQ[26]/DDR0_DQ[58]
DDR1_DQ[27]/DDR0_DQ[59]
DDR1_DQ[28]/DDR0_DQ[60]
DDR1_DQ[29]/DDR0_DQ[61]
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DDR1_DQ[31]/DDR0_DQ[63]
DDR1_DQ[32]/DDR1_DQ[16]
DDR1_DQ[33]/DDR1_DQ[17]
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DDR1_DQ[36]/DDR1_DQ[20]
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DDR1_DQ[40]/DDR1_DQ[24]
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DDR1_DQ[42]/DDR1_DQ[26]
DDR1_DQ[43]/DDR1_DQ[27]
DDR1_DQ[44]/DDR1_DQ[28]
DDR1_DQ[45]/DDR1_DQ[29]
DDR1_DQ[46]/DDR1_DQ[30]
DDR1_DQ[47]/DDR1_DQ[31]
DDR1_DQ[48]
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DDR1_DQ[51]
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DDR1_DQ[53]
DDR1_DQ[54]
DDR1_DQ[55]
DDR1_DQ[56]
DDR1_DQ[57]
DDR1_DQ[58]
DDR1_DQ[59]
DDR1_DQ[60]
DDR1_DQ[61]
DDR1_DQ[62]
DDR1_DQ[63]
DDR1_ECC[0]
DDR1_ECC[1]
DDR1_ECC[2]
DDR1_ECC[3]
DDR1_ECC[4]
DDR1_ECC[5]
DDR1_ECC[6]
DDR1_ECC[7]

DDR CHANNEL B

BIOSTAR-D
SKYLAKE-S
Rev:0.7

DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]

DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_BA[1]/DDR1_CAB[5]/DDR1_BA[1]
DDR1_BA[2]/DDR1_CAB[5]/DDR1_BG[0]

DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
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DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]
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DDR1_QOSP[5]/DDR1_QOSP[3]
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DDR1_QOSP[7]

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DDR1_QOSP[8]

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DDR1_VREF_DQ

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DDR1_ODT[0]
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DDR1_MAA_B13

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DDR1_MAA_B13

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DDR1_MAA_B3
DDR1_MAA_B4
DDR1_MAA_B5
DDR1_MAA_B6
DDR1_MAA_B7
DDR1_MAA_B8
DDR1_MAA_B9
DDR1_MAA_B10
DDR1_MAA_B11
DDR1_MAA_B12
DDR1_MAA_B13

DDR1_MAA_B0
DDR1_MAA_B1
DDR1_MAA_B2
DDR1_MAA_B3
DDR1_MAA_B4
DDR1_MAA_B5
DDR1_MAA_B6
DDR1_MAA_B7
DDR1_MAA_B8
DDR1_MAA_B9
DDR1_MAA_B10
DDR1_MAA_B11
DDR1_MAA_B12
DDR1_MAA_B13

AM20 >>> CK_M_CH1_0_DP 12
AM21 >>> CK_M_CH1_0_DN 12
AP22 >>> CK_M_CH1_1_DP 12
AP21 >>> CK_M_CH1_1_DN 12

AN20 >>> M_SCKE_B0 12
AN21 >>> M_SCKE_B1 12
AP19 >>> M_SCS_B_N0 12
AP20 >>> M_SCS_B_N1 12

AY29 >>> M_ODT_B0 12
AV29 >>> M_ODT_B1 12
AW29 >>> M_ODT_B1 12
AU29 >>> M_ODT_B1 12

AP17 >>> M_ODT_B0 12
AN15 >>> M_ODT_B1 12
AN17 >>> M_ODT_B1 12
AM15 >>> M_ODT_B1 12

AL16 >>> M_ODT_B0 12
AL16 >>> M_ODT_B1 12
AP15 >>> M_ODT_B1 12
AL15 >>> M_ODT_B1 12

AN18 >>> M_MAA_B[0..16] 12
AL17 >>> M_MAA_B[0..16] 12
AP16 >>> M_MAA_B[0..16] 12

AL18 >>> M_SBS_B0 12
AM18 >>> M_SBS_B1 12
AW28 >>> M_BG_CH1_0 12

AL19 >>> M_MAA_B0 12
AL22 >>> M_MAA_B1 12
AM22 >>> M_MAA_B2 12
AM23 >>> M_MAA_B3 12
AP23 >>> M_MAA_B4 12
AW23 >>> M_MAA_B5 12
AY26 >>> M_MAA_B6 12
AU26 >>> M_MAA_B7 12
AW27 >>> M_MAA_B8 12
AP18 >>> M_MAA_B9 12
AU27 >>> M_MAA_B10 12
AU27 >>> M_MAA_B11 12
AV27 >>> M_MAA_B12 12
AR15 >>> M_MAA_B13 12

AY28 >>> M_BG_CH1_1 12
AU28 >>> M_BG_CH1_1 12

AL20 >>> M_BG_CH1_1 12
AY25 >>> M_BG_CH1_1 12

AF34 >>> M_DQS_B_DN0 12
AK33 >>> M_DQS_B_DN1 12
AN33 >>> M_DQS_B_DN2 12
AN29 >>> M_DQS_B_DN3 12
AN13 >>> M_DQS_B_DN4 12
AR8 >>> M_DQS_B_DN5 12
AM8 >>> M_DQS_B_DN6 12
AG6 >>> M_DQS_B_DN7 12

AF35 >>> M_DQS_B_DP0 12
AL33 >>> M_DQS_B_DP1 12
AP33 >>> M_DQS_B_DP2 12
AN28 >>> M_DQS_B_DP3 12
AN12 >>> M_DQS_B_DP4 12
AP8 >>> M_DQS_B_DP5 12
AL8 >>> M_DQS_B_DP6 12
AG7 >>> M_DQS_B_DP7 12

AN25 >>> M_DQS_B_DP8 12
AN26 >>> M_DQS_B_DP9 12

AB40 >>> M_DQS_B_DP10 12
AC40 >>> M_DQS_B_DP11 12
AC39 >>> M_DQS_B_DP12 12

AB40 >>> M_DQS_B_DP10 12
AC40 >>> M_DQS_B_DP11 12
AC39 >>> M_DQS_B_DP12 12

AB40 >>> M_DQS_B_DP10 12
AC40 >>> M_DQS_B_DP11 12
AC39 >>> M_DQS_B_DP12 12

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AC40 >>> M_DQS_B_DP11 12
AC39 >>> M_DQS_B_DP12 12

AB40 >>> M_DQS_B_DP10 12
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AB40 >>> M_DQS_B_DP10 12
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AC39 >>> M_DQS_B_DP12 12

AB40 >>> M_DQS_B_DP10 12
AC40 >>> M_DQS_B_DP11 12
AC39 >>> M_DQS_B_DP12 12

AB40 >>> M_DQS_B_DP10 12
AC40 >>> M_DQS_B_DP11 12
AC39 >>> M_DQS_B_DP12 12

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AC40 >>> M_DQS_B_DP11 12
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AB40 >>> M_DQS_B_DP10 12
AC40 >>> M_DQS_B_DP11 12
AC39 >>> M_DQS_B_DP12 12

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DDR CH1 ALERT N

DDR VREF CA

DDR0 VREF DQ

DDR1 VREF DQ

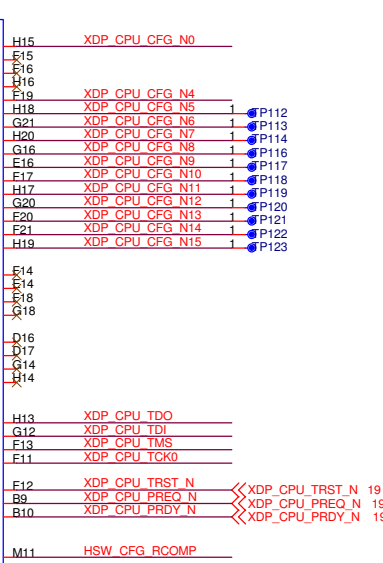
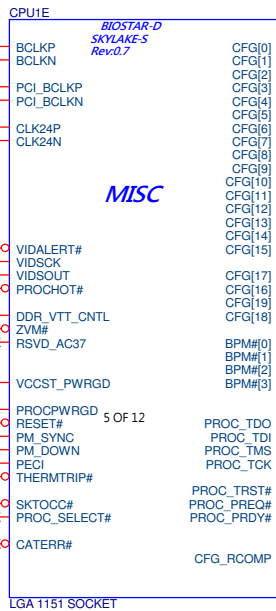
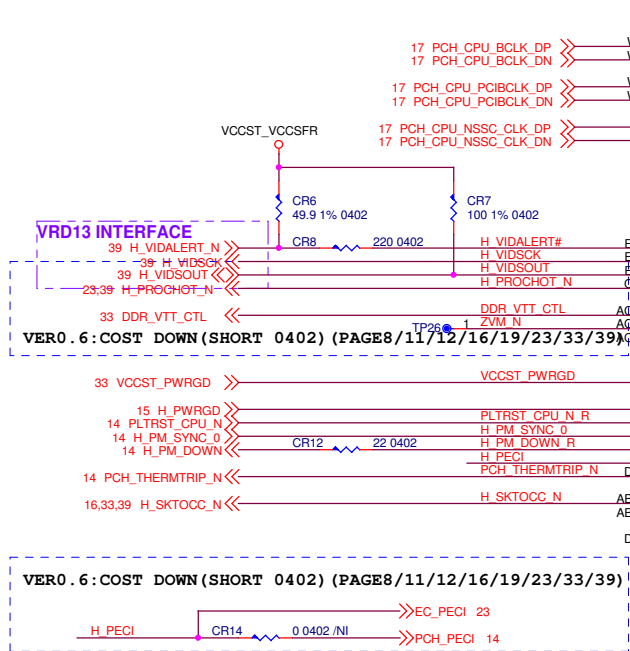


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Title CPU DDR3 CHANNEL B

Size B Document Number IH11K-MHS Rev 6.1

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CFG	HIGH	LOW	STRAP DESCRIPTION
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG_UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVATE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI_AC_COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYN	PMSYNC ASYN MODE
14	RESERVED		
15	RESERVED		

ALL PINS HAVE INTERNAL PULL-UPS

Bifurcation	Link Width			Config. Signals		
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]
1x16	x16	N/A	N/A	1	1	1
1x16 Reversed	x16	N/A	N/A	1	1	0
2x8	x8	x8	N/A	1	0	1
2x8 Reversed	x8	x8	N/A	1	0	0
1x8+2x4	x8	x4	x4	0	0	1
1x8+2x4 Reversed	x8	x4	x4	0	0	0

Configuration Signals: The CFG signals have a default value of '1'. If not terminated on the board, refer to the appropriate platform design guide for pull-downs. (Refer to comments placing test points on the board for CFG pins.)

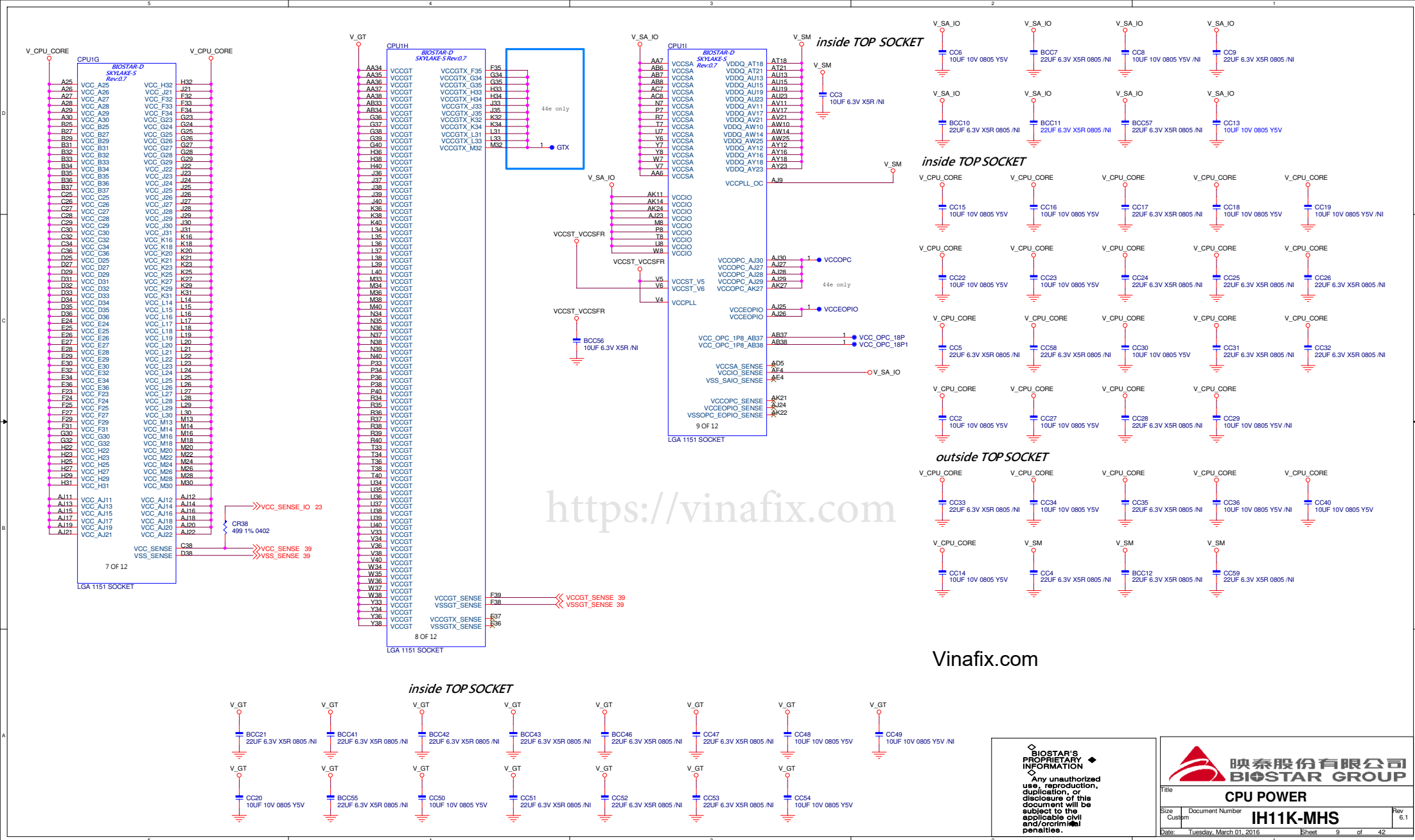
- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted.
 - 1 = (Configured) Normal Operation;
 - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Reversal.
 - 1 = Normal operation.
 - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable.
 - 1 = Disabled.
 - 0 = Enabled.
- **CFG[5]**: PCI Express* Bifurcation.
 - 00 = 1 x8, 2 x8 PCI Express* reserved.
 - 01 = 2 x8 PCI Express* reserved.
 - 10 = 1 x16 PCI Express* reserved.
 - 11 = 1 x16 PCI Express* reserved.
- **CFG[7]**: PEG Training.
 - 1 = (Default) PEG Training immediately following RESET# de-assertion.
 - 0 = PEG Wait for BIOS for training.
- **CFG[10:15]**: Reserved configuration lanes.

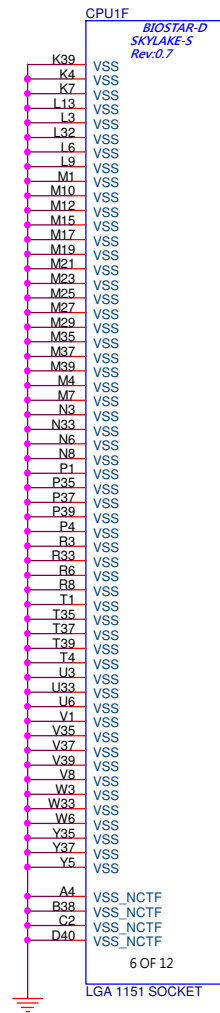
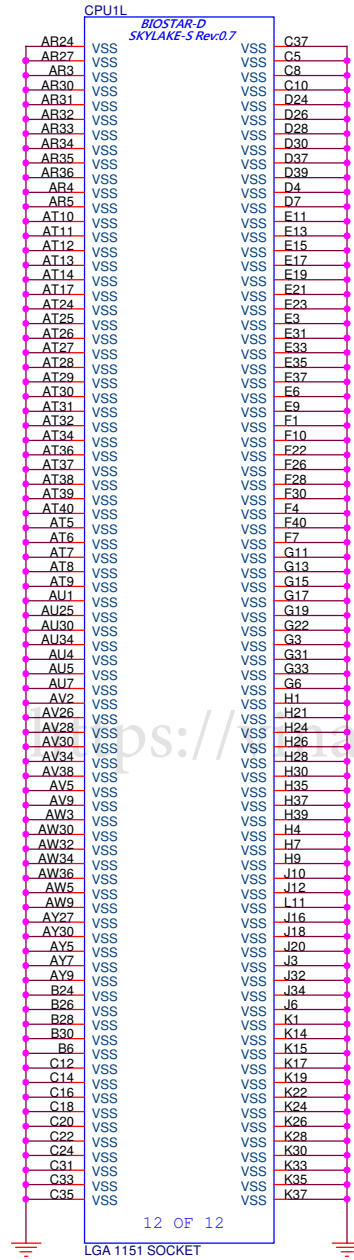
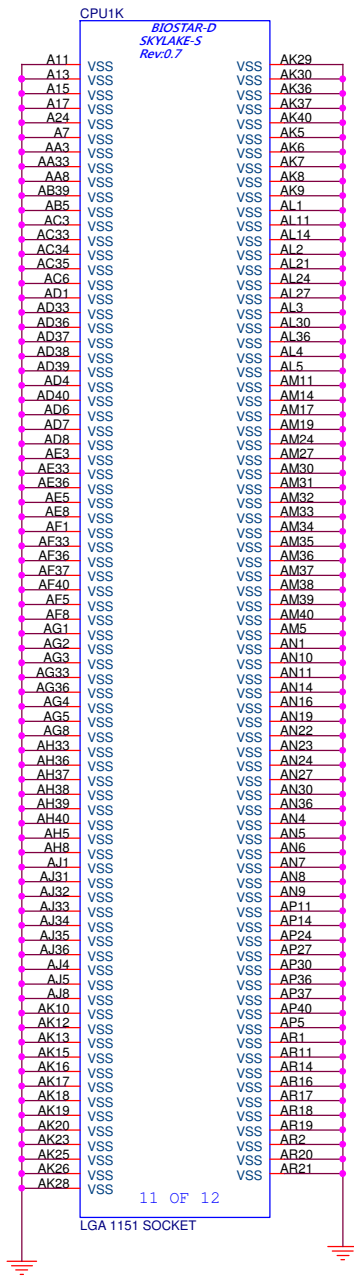
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CPU MISC

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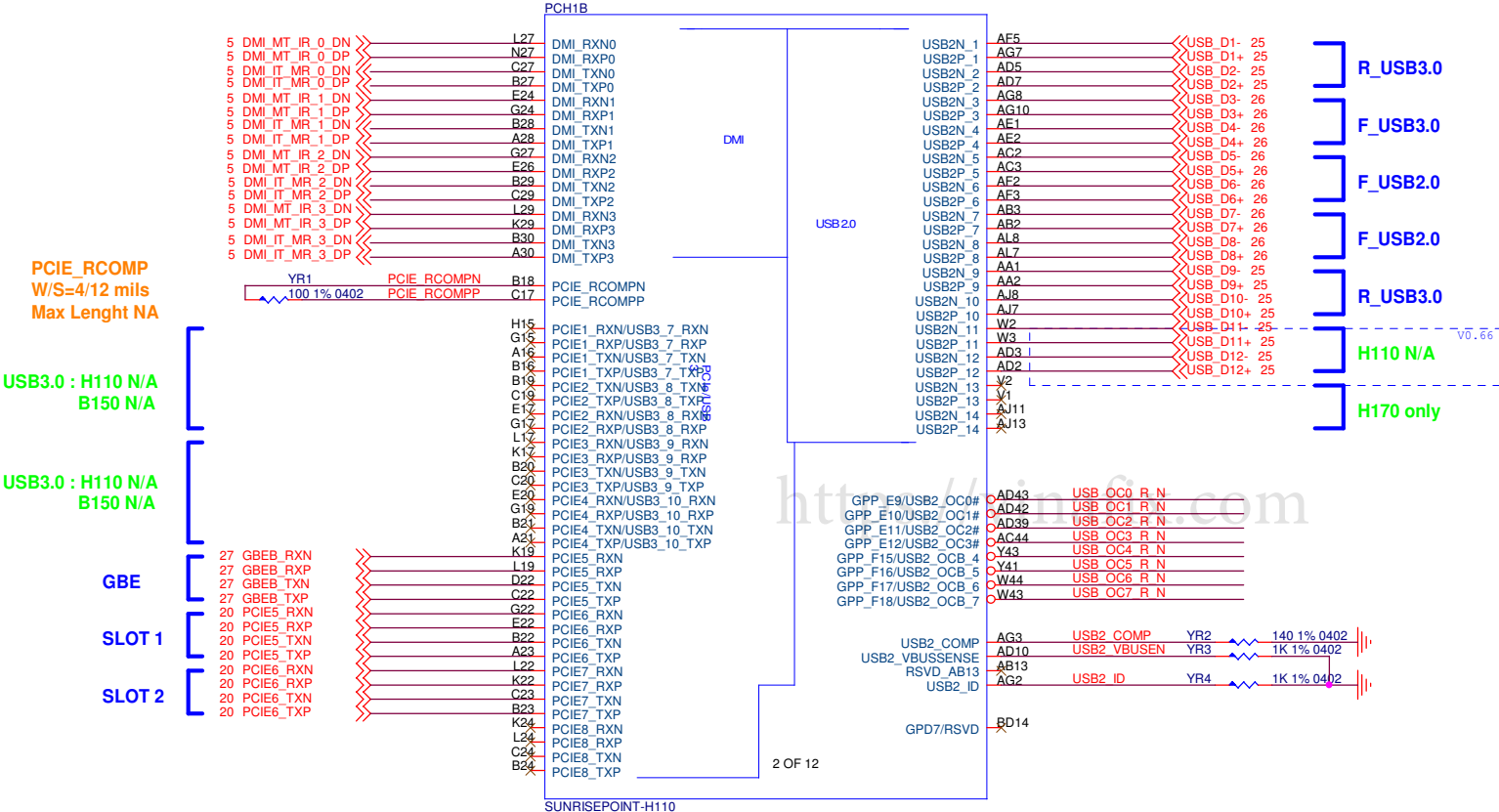
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PCH PART: Y+Reference



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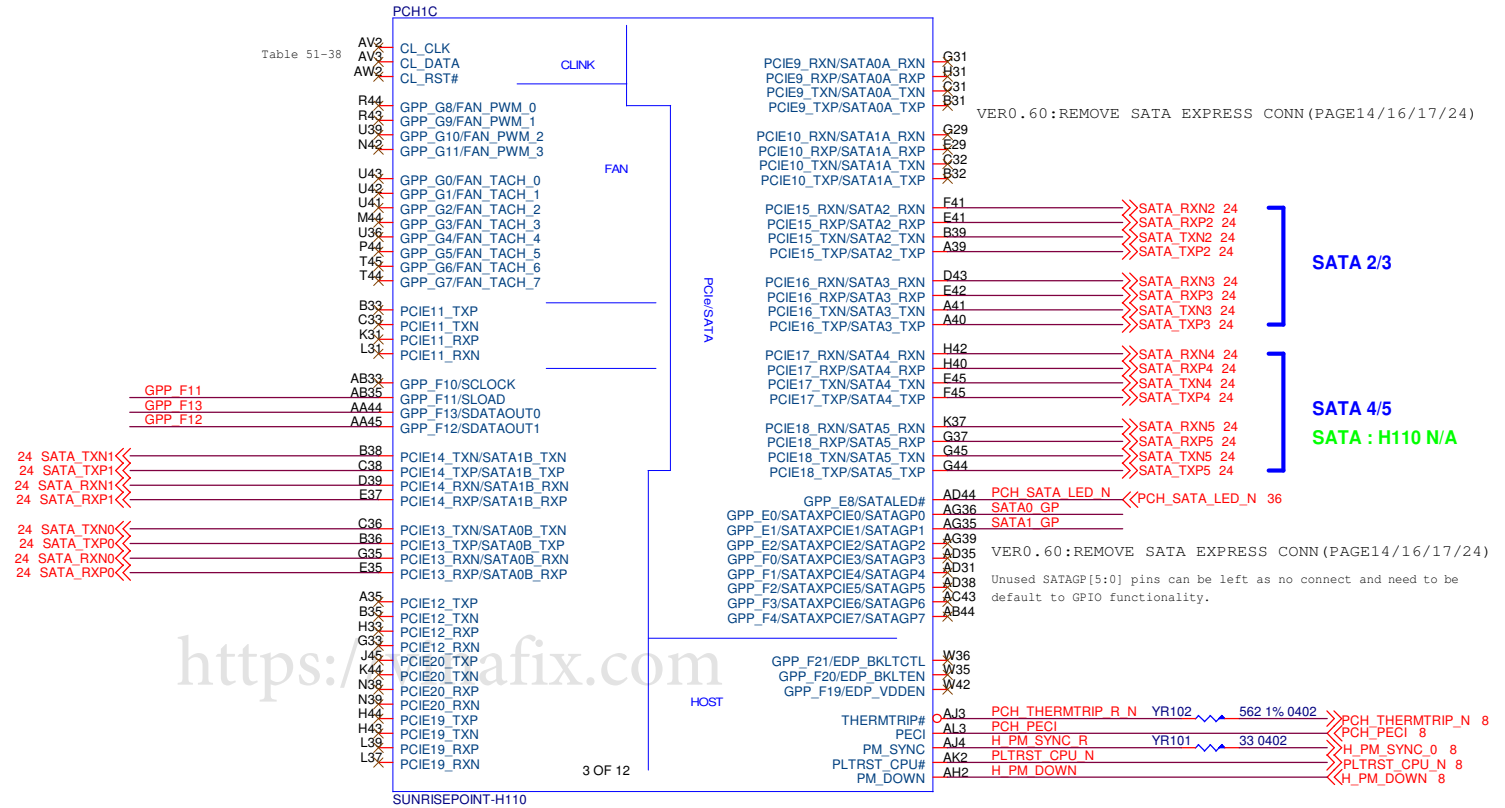
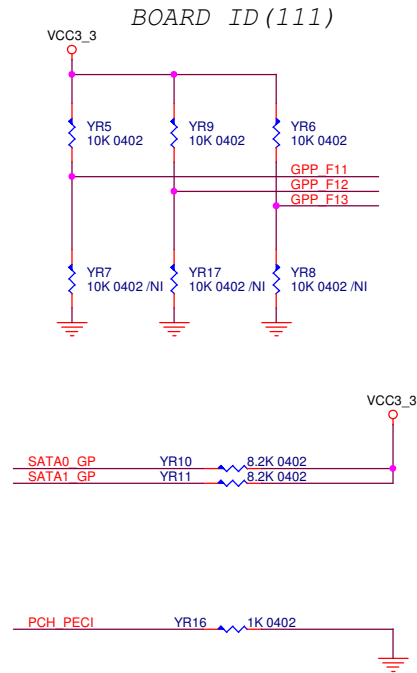
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PCH PART: Y+Reference



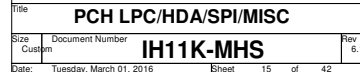
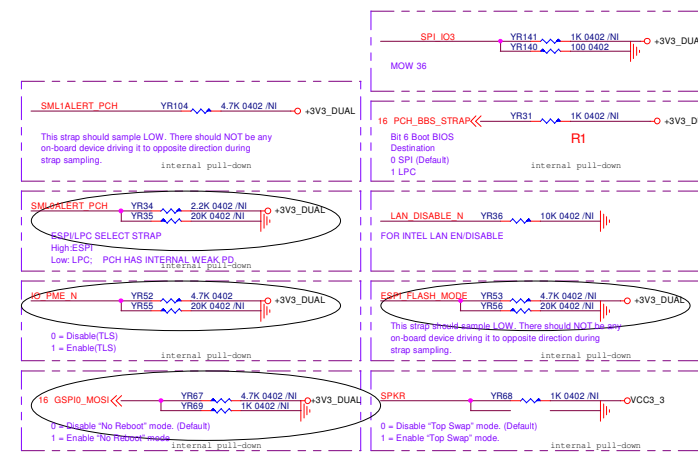
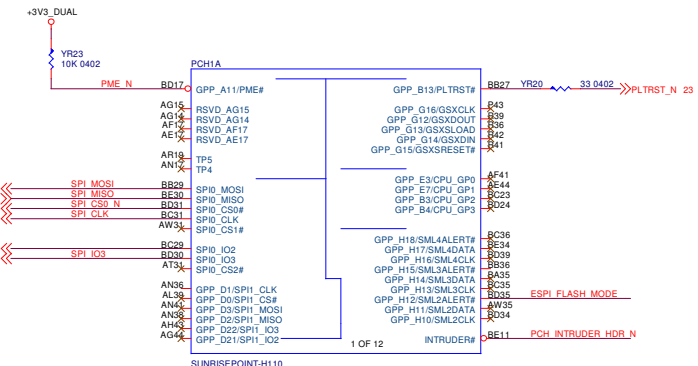
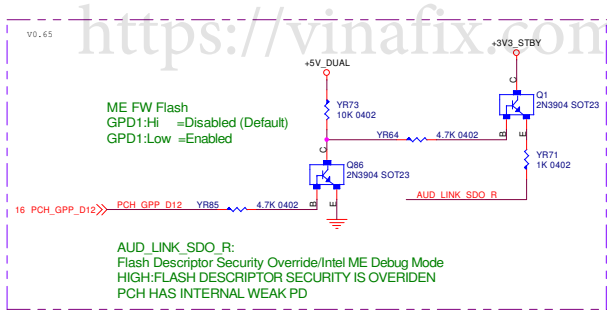
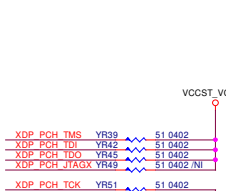
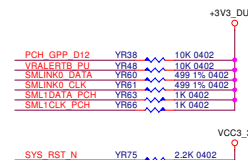
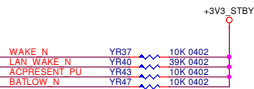
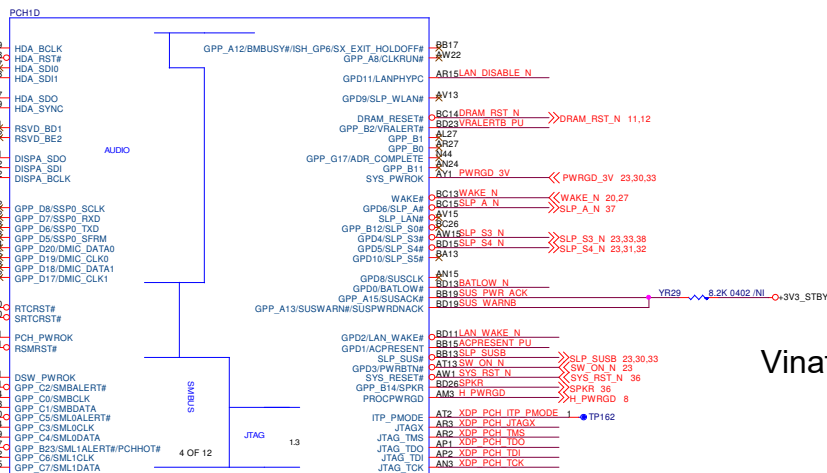
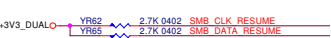
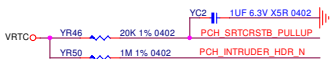
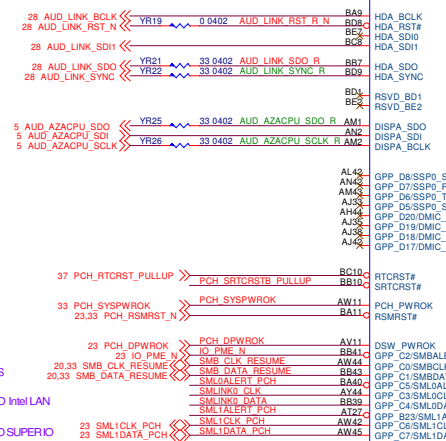
GbE can be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13.

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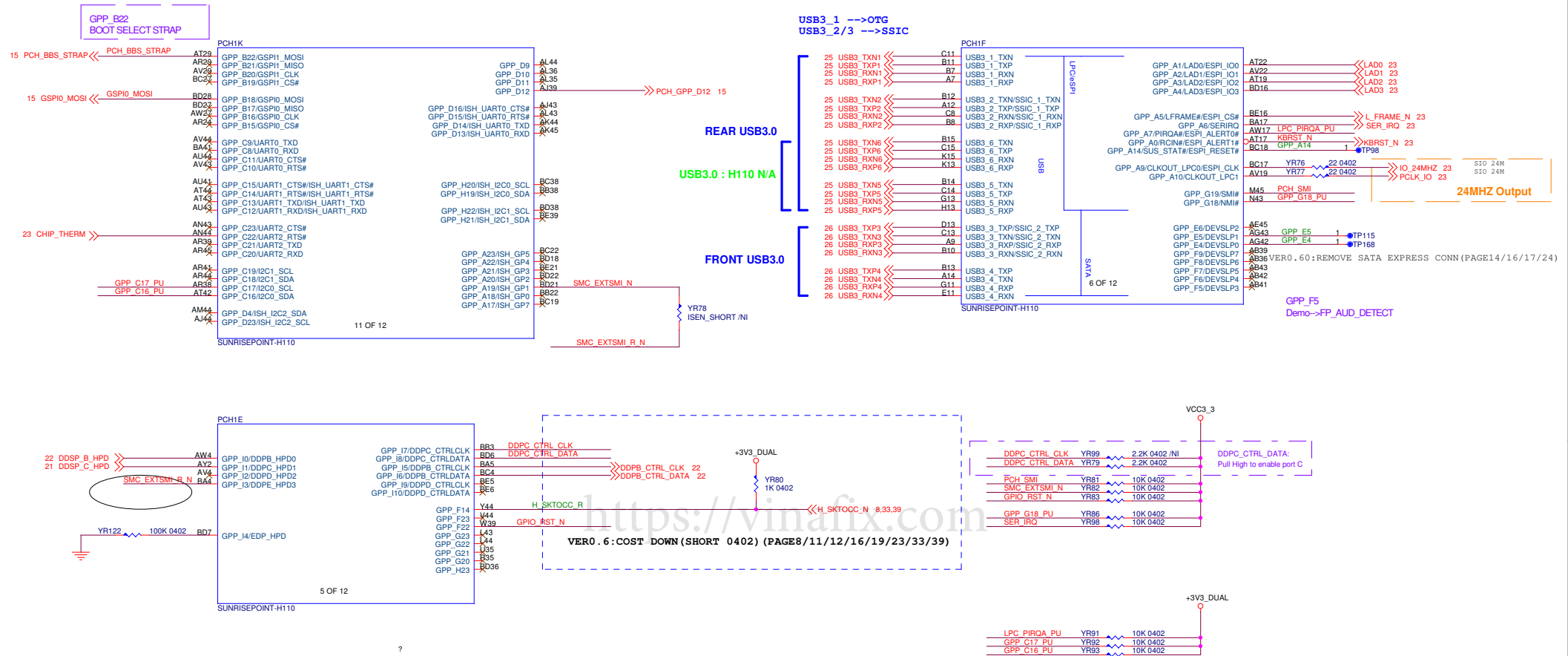
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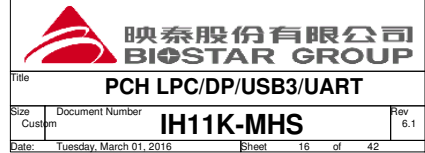


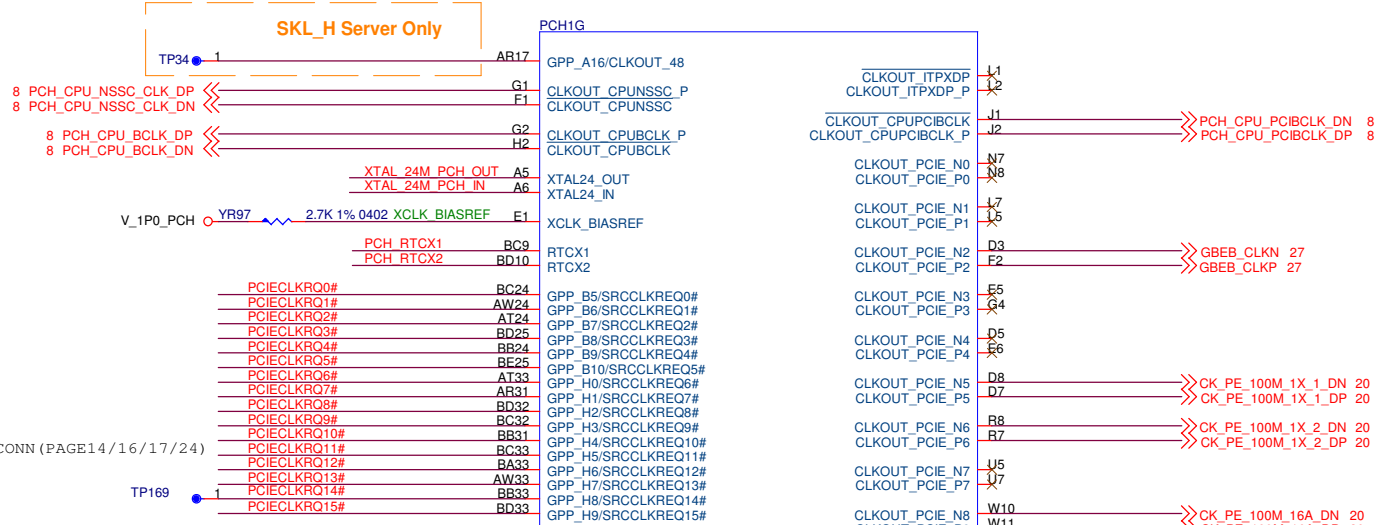
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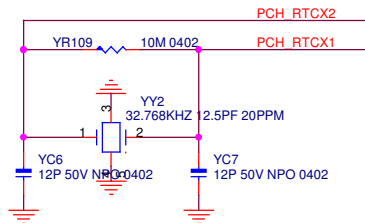
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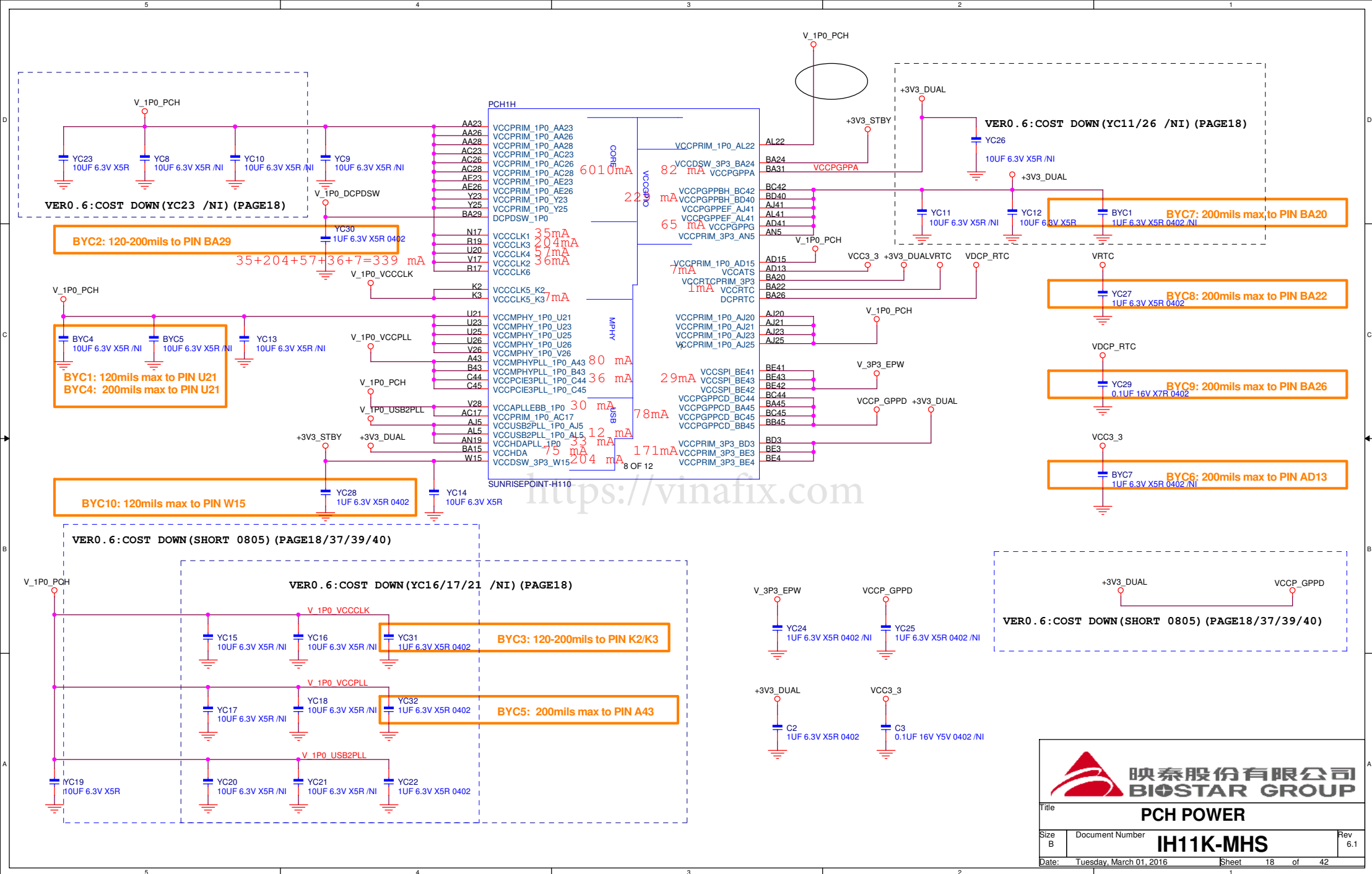


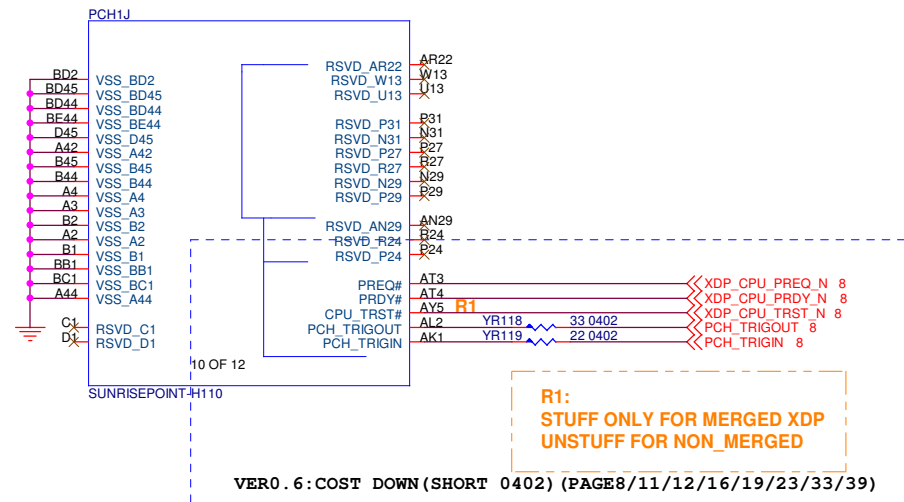
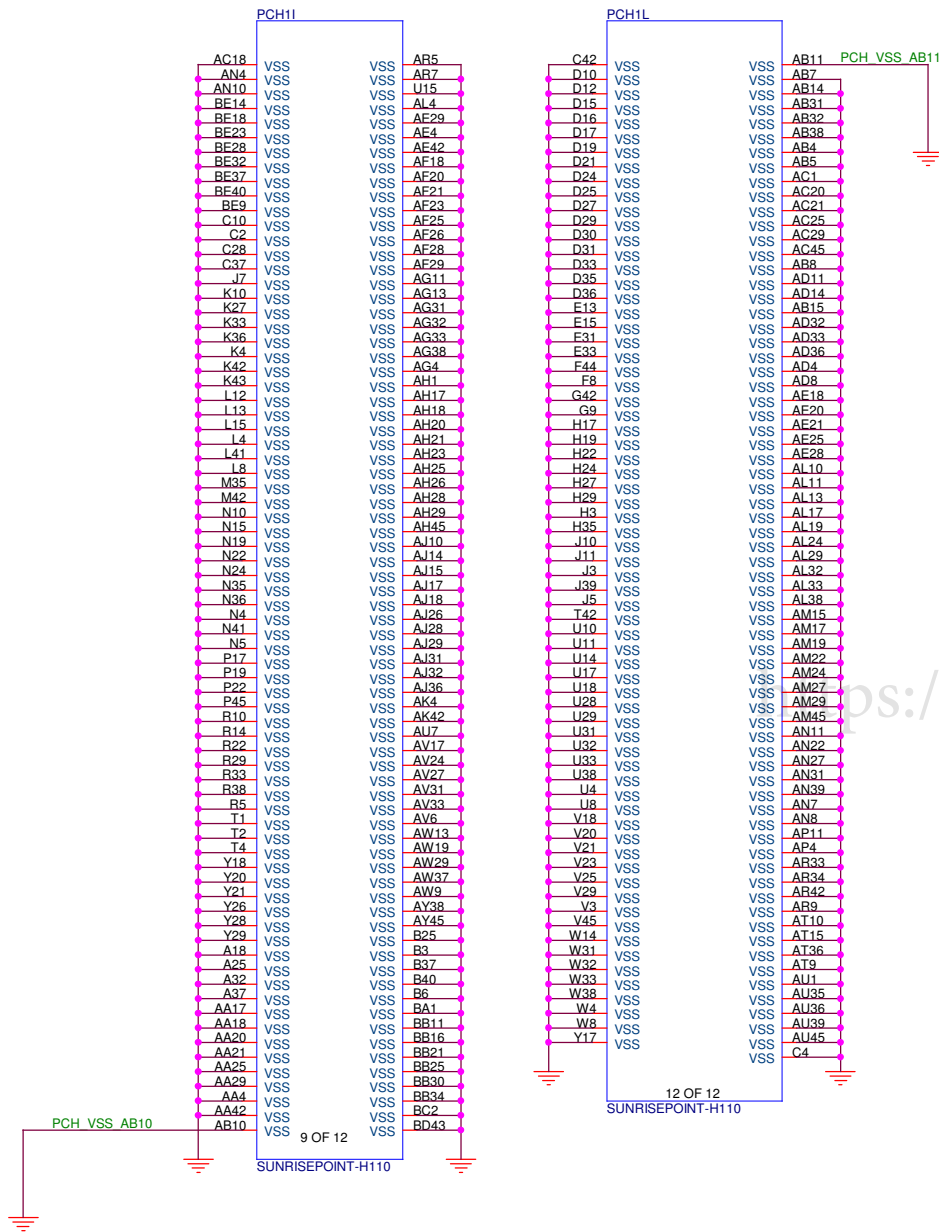
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RTC CRYSTAL



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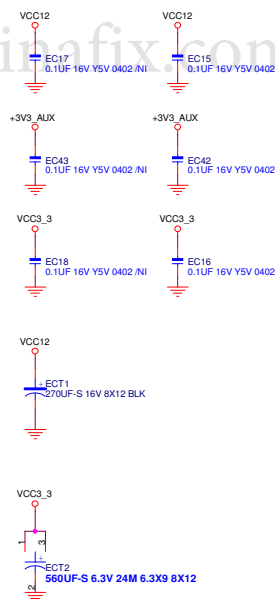
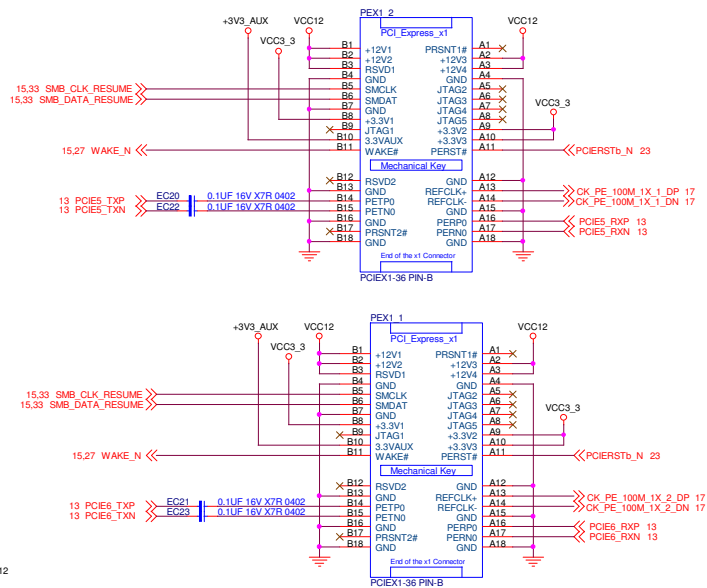
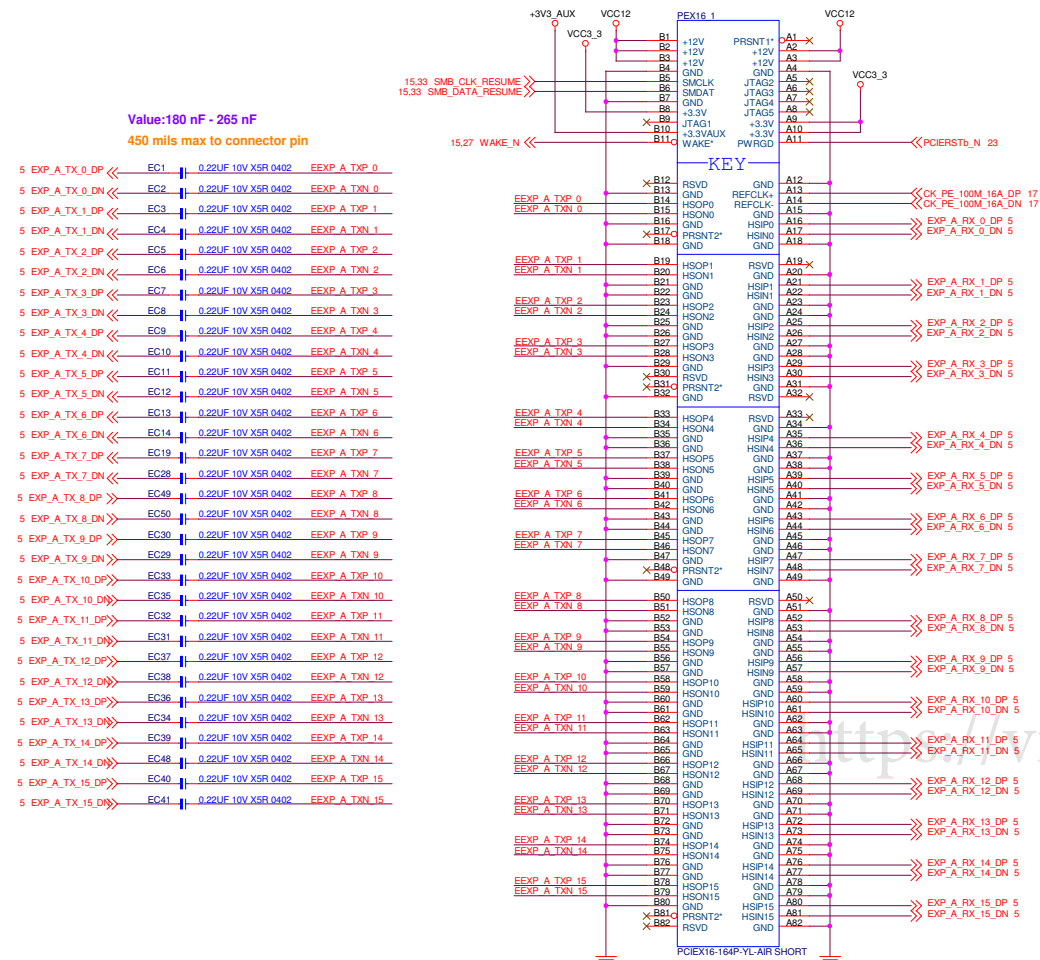




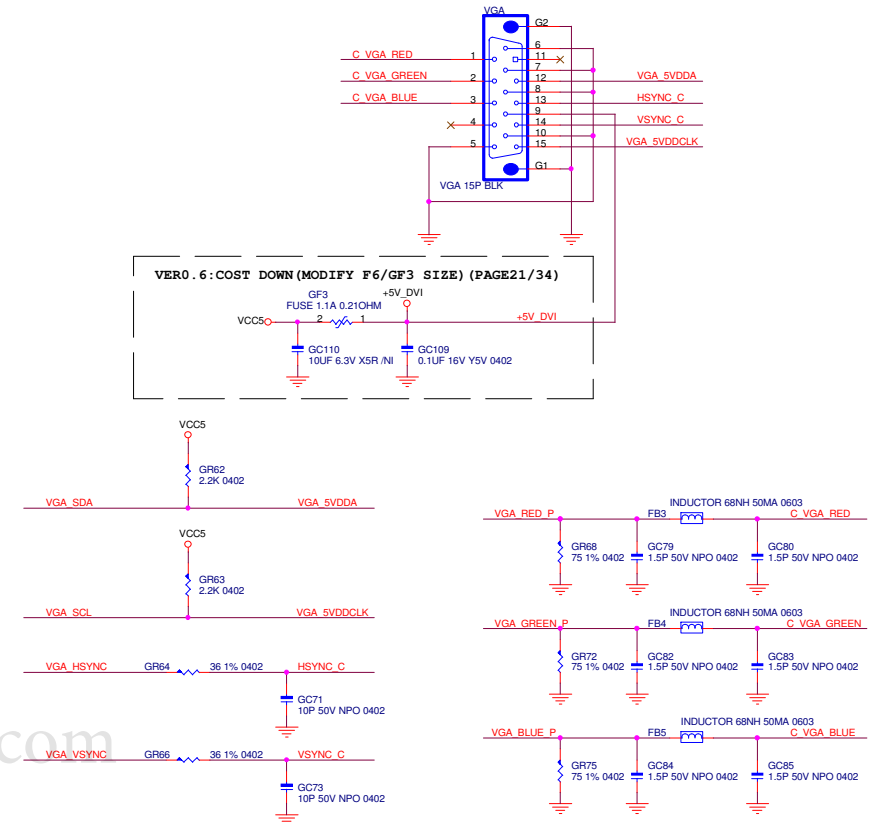
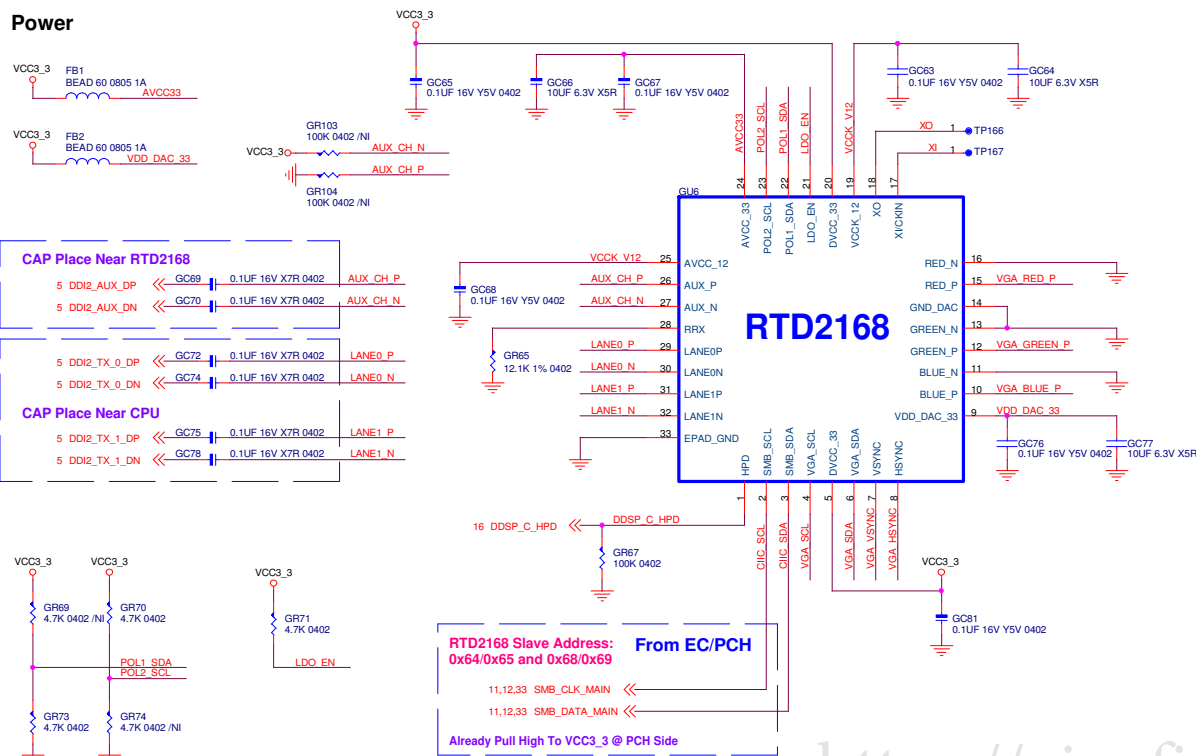
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SLOT PART: E+Reference



Power



Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EPPROM MODE

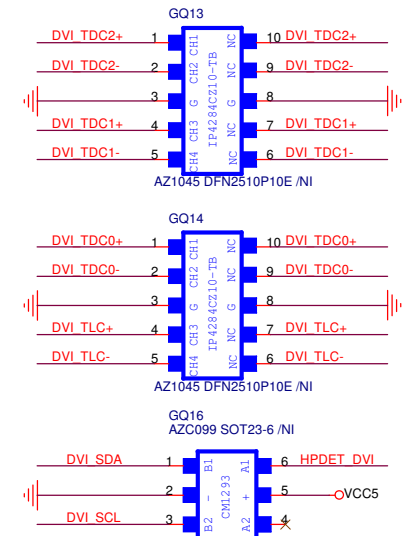
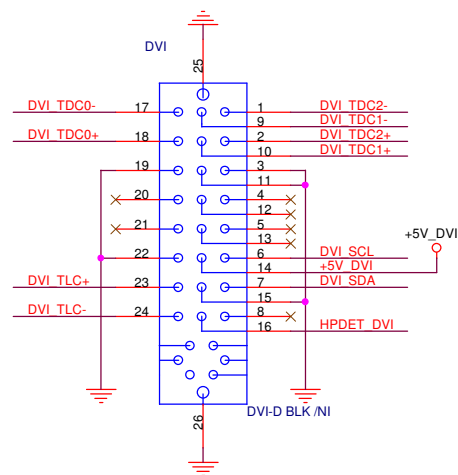
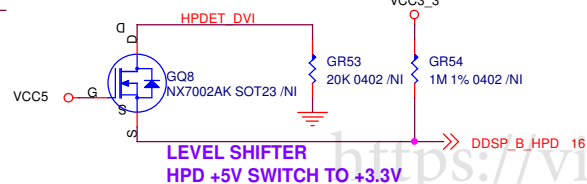
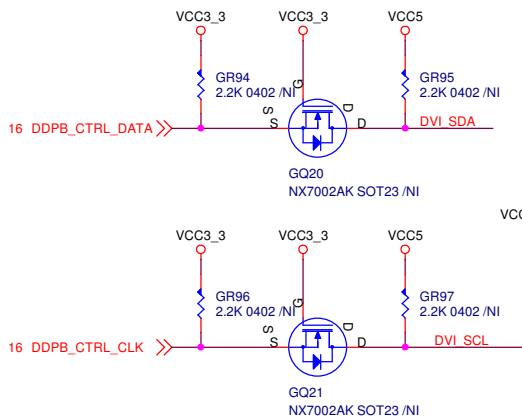
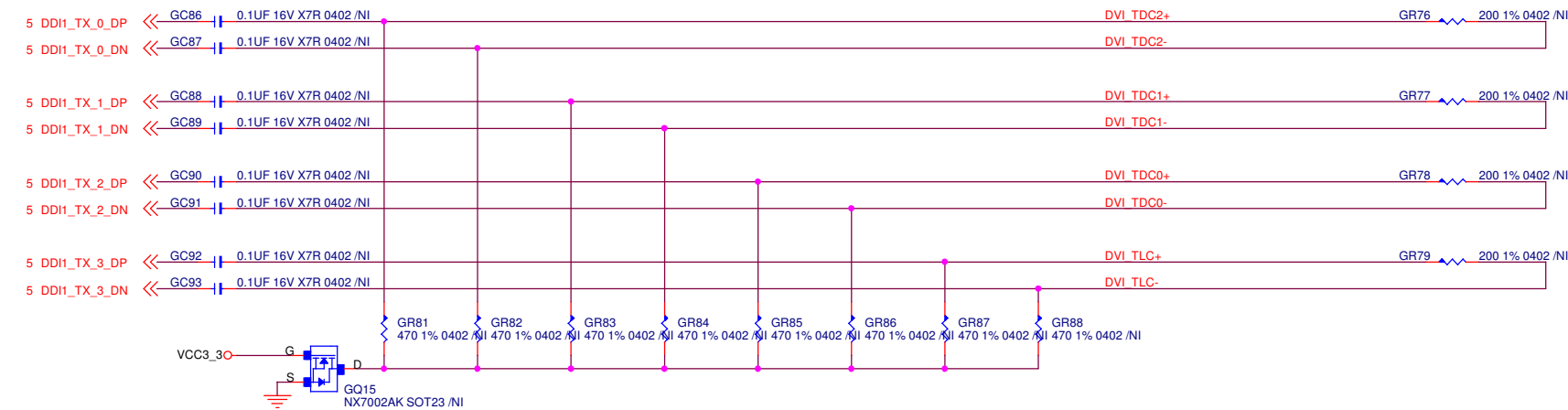
Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

Table 12 Power consumption by using embedded LDO and embedded clock source

Active Resolution / Standby	DP Config.	Min	Typ	Max	Unit
1280x800x60(74.25-MHz)	1-Lane	-	400	450	mW
1600x900x60(103-MHz)	1-Lane	-	420	480	mW
1920x1080x60(148-MHz)	2-Lane	-	480	595	mW
Stand-by mode	-	-	7.5	8	mW



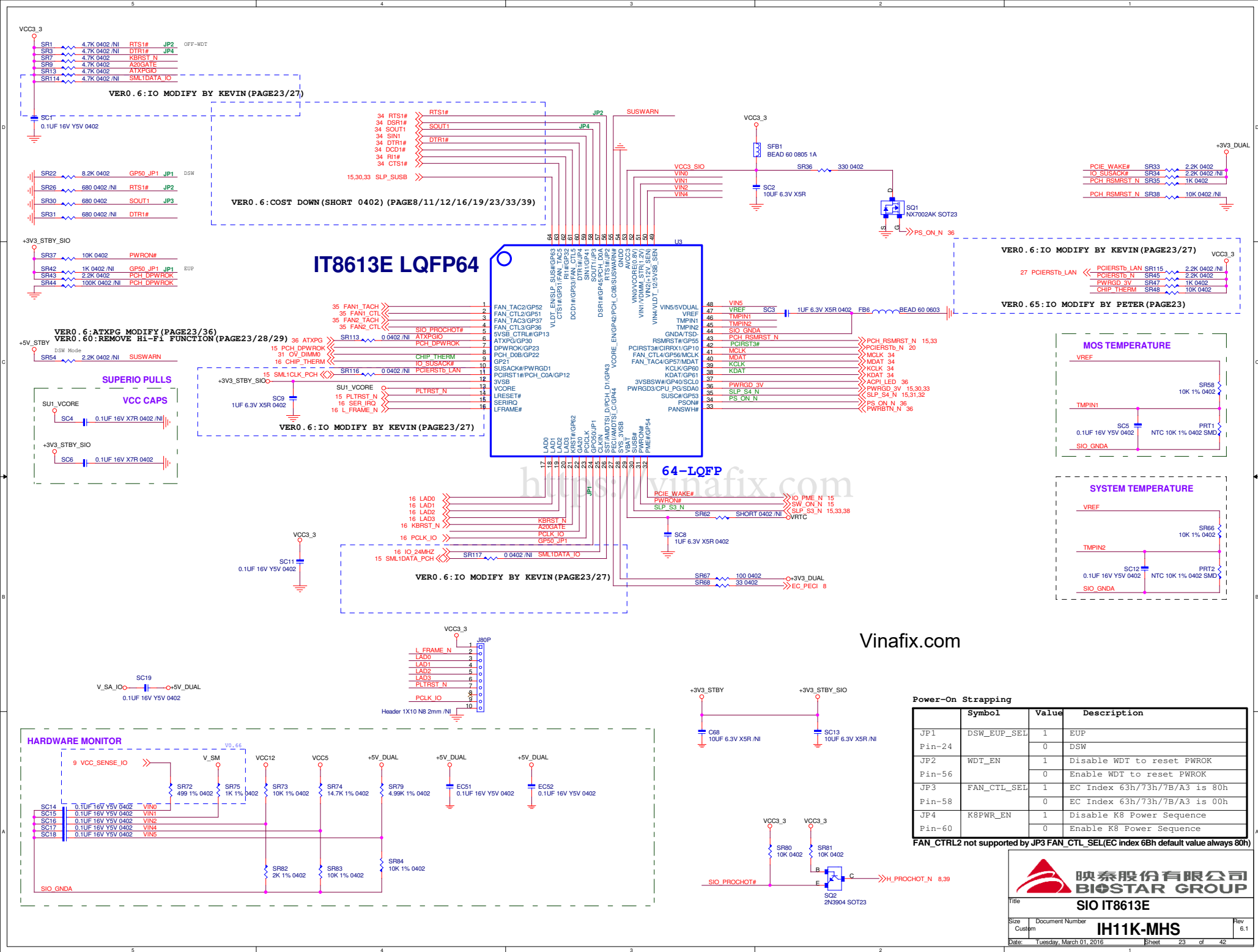


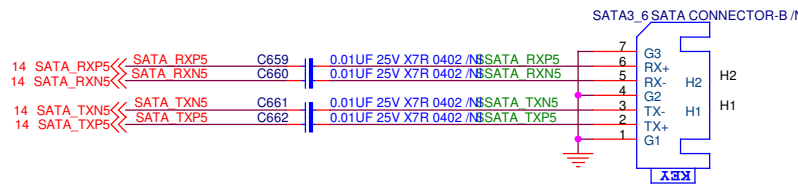
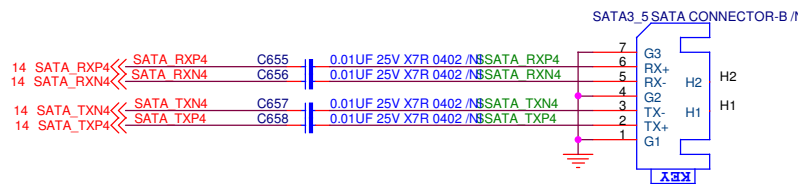
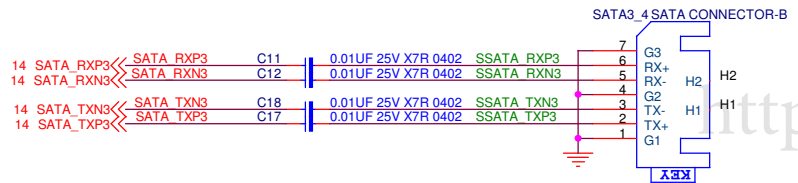
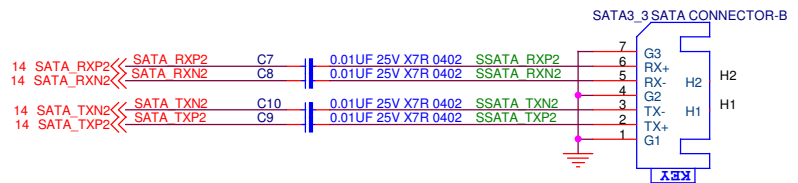
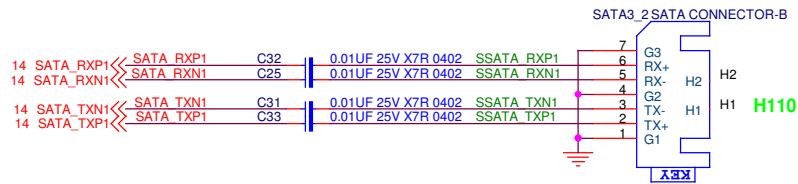
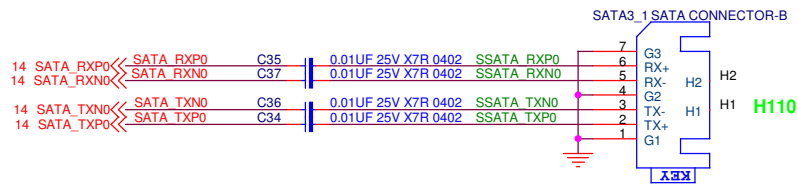
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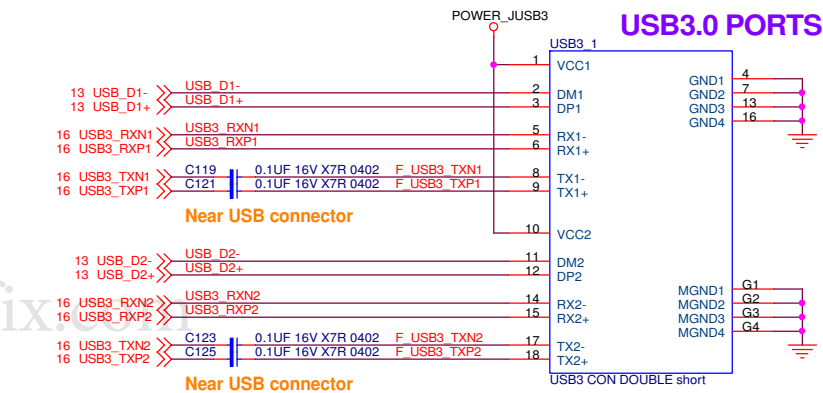
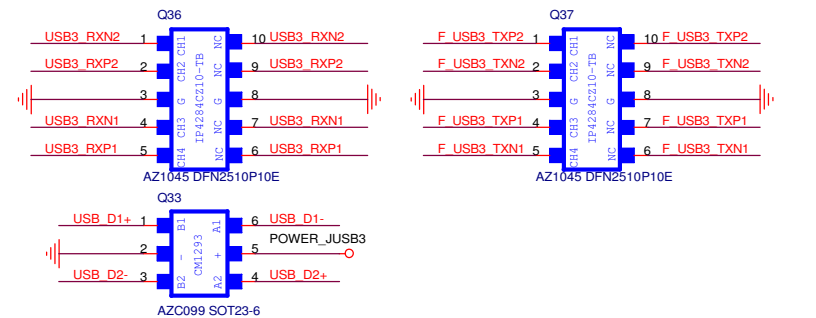


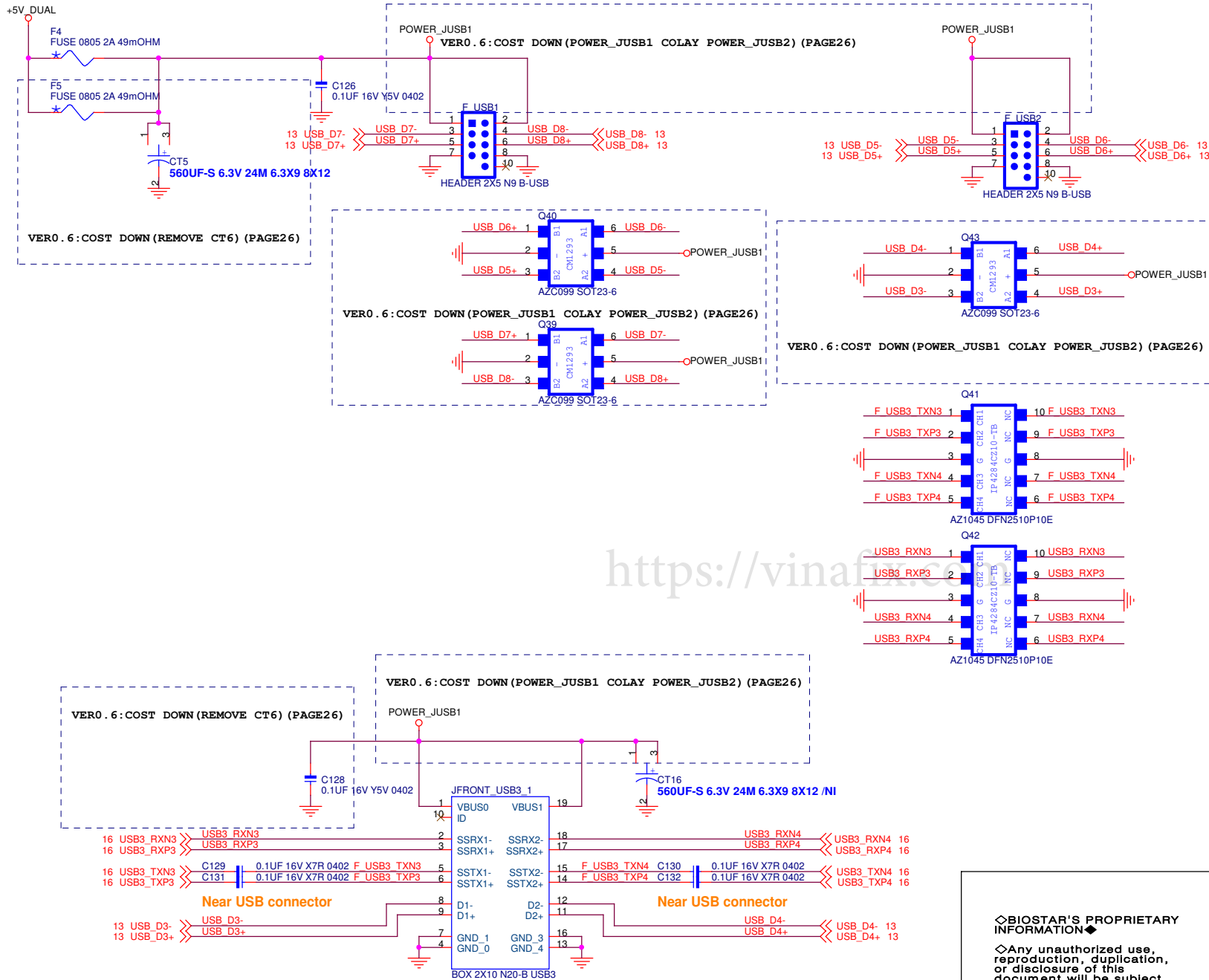
VER0.65:NEW ADD SATA CONN (PAGE14/24)

VER0.60:REMOVE SATA EXPRESS CONN (PAGE14/16/17/24)

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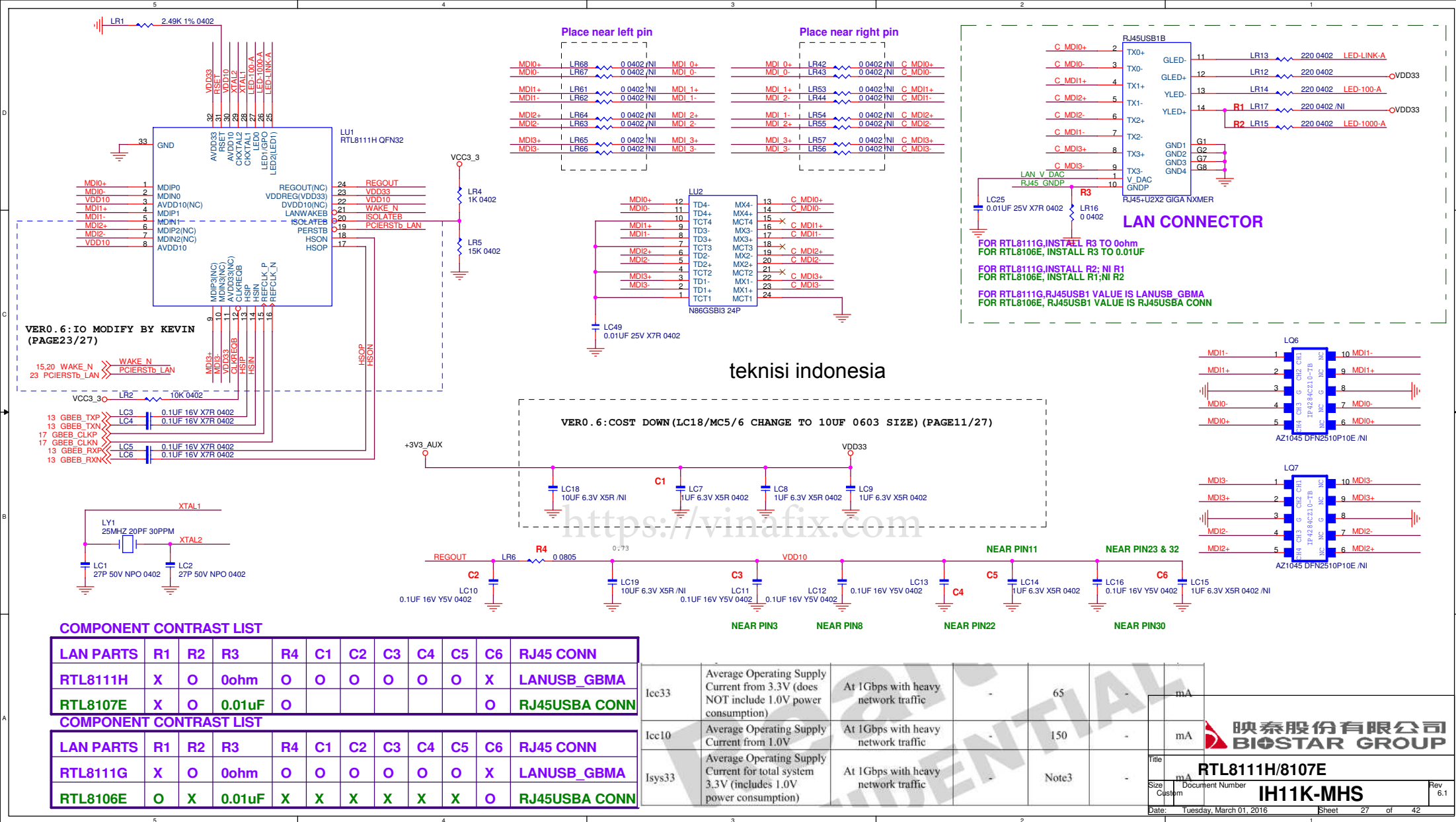


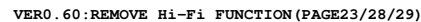
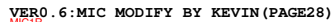
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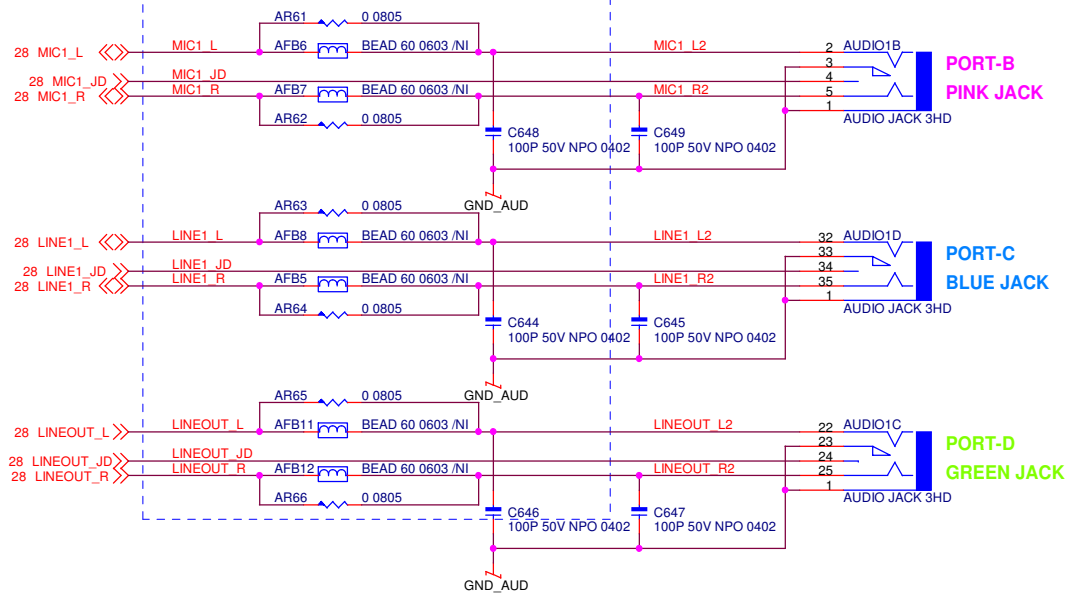
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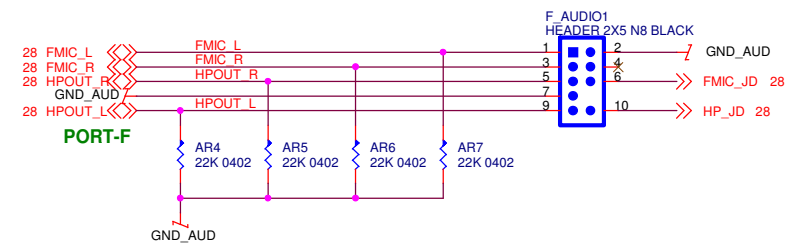


REAR AUDIO JACKS

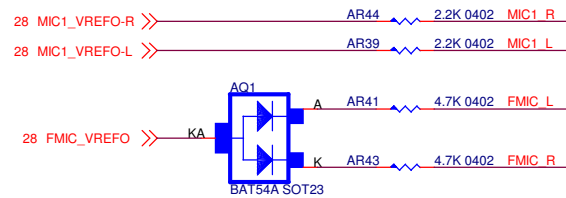
VER0.6: COST DOWN (BEAD COLAY) (PAGE 29)



FRONT AUDIO HEADER



MIC VREF

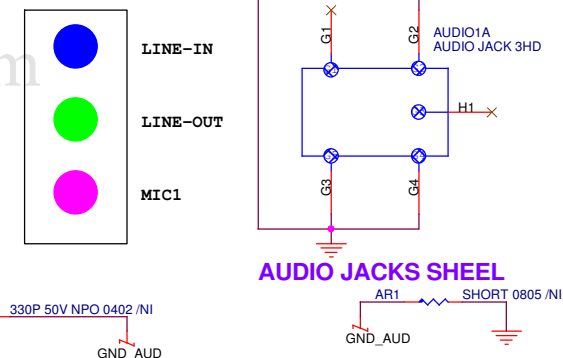


SPDIF CONNECTOR

V0.66

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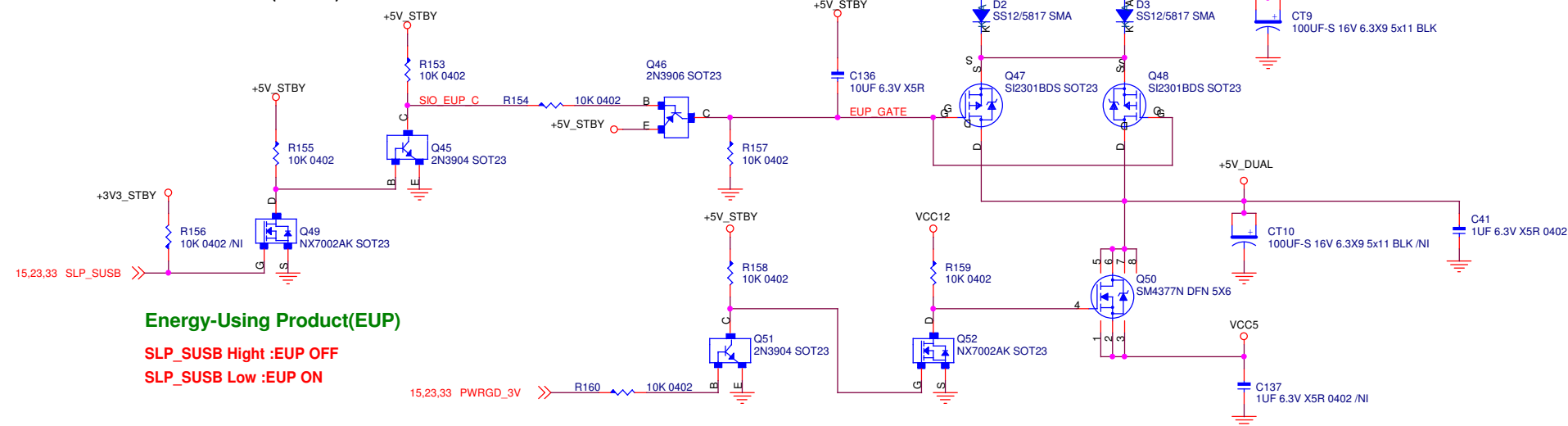
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Title: AUDIO CONNECTOR

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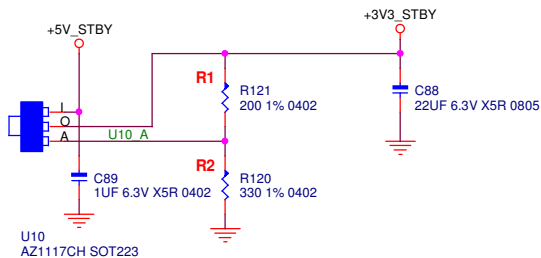
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VER0.6:ACPI MODIFY BY KEVIN(PAGE30)

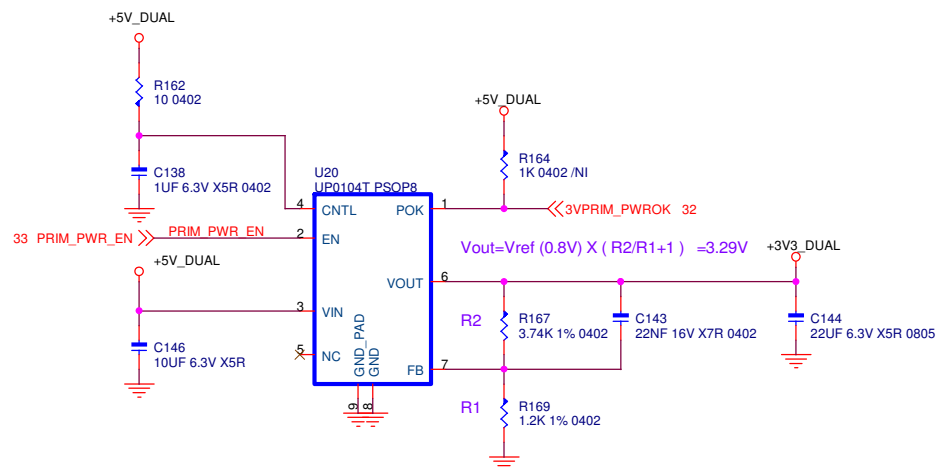
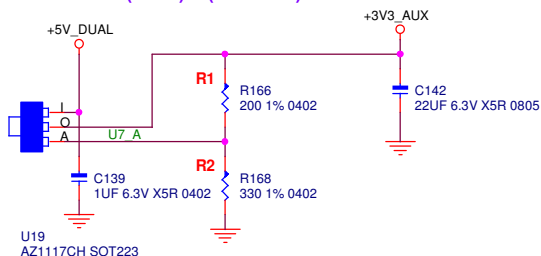


VER0.6:COST DOWN(2N7002 CHANGE TO 2N3904) (PAGE30/33/39)

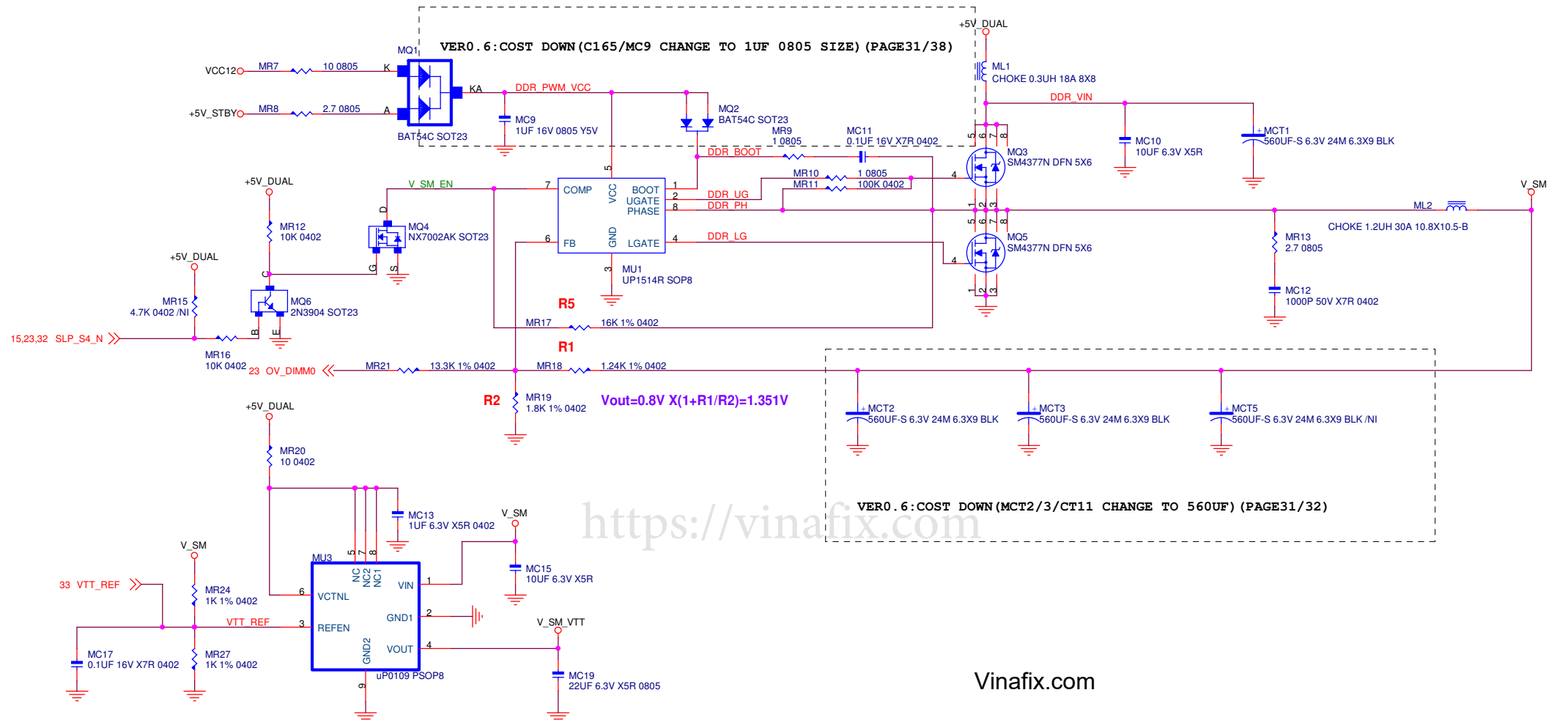
$$V_{out}=V_{ref} (1.25V) \times (1+R2/R1)=3.3125V$$



$$V_{out}=V_{ref} (1.25V) \times (1+R2/R1)=3.3125V$$




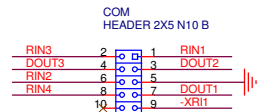
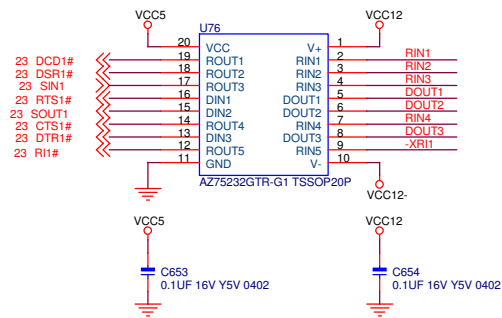
MEMORY PART:M+Reference



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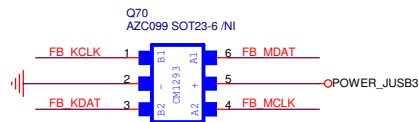
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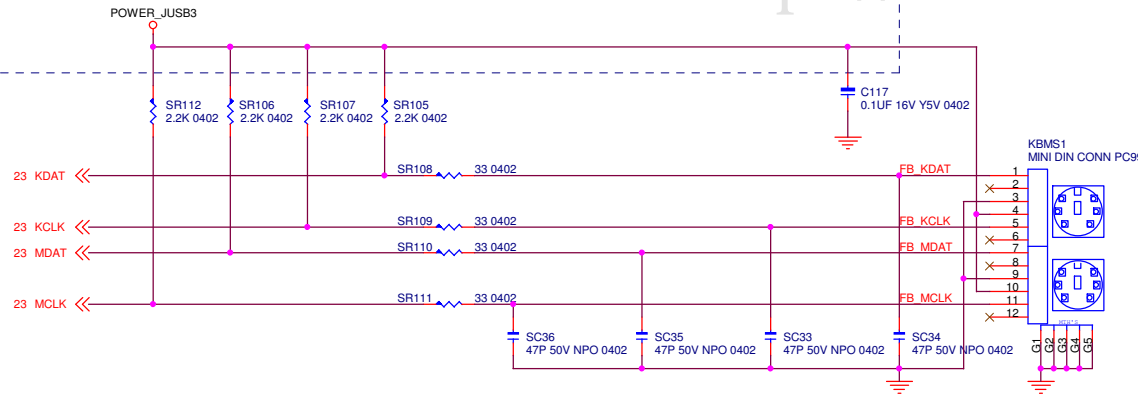
COM PORT

WAKE ON RING



KEYBOARD & MOUSE

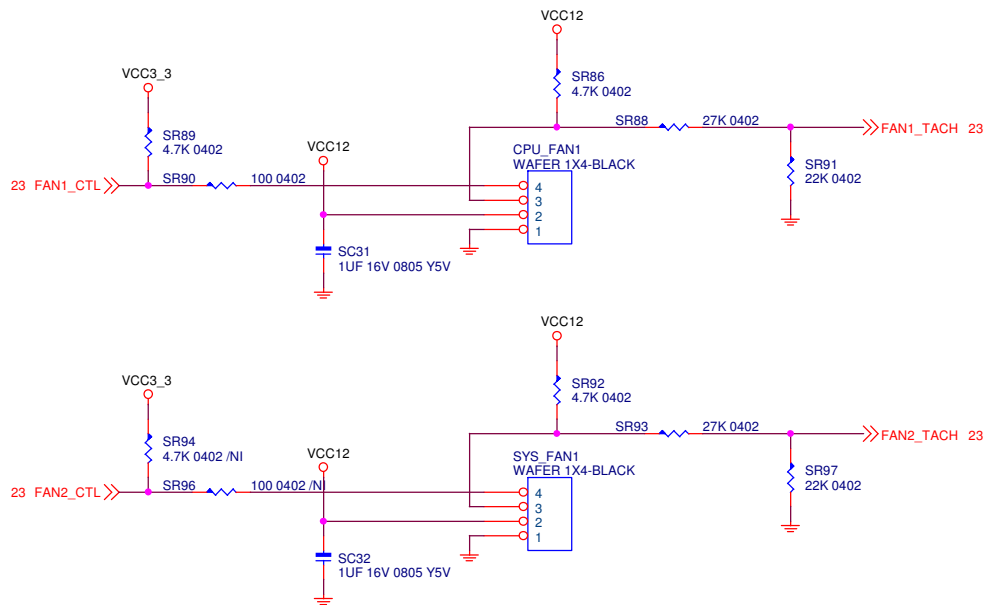
VER0.6: COST DOWN (POWER_JUSB4/POWER_JUSB5 COLAY) (PAGE25/34)



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COM1 / PS2 CONN	
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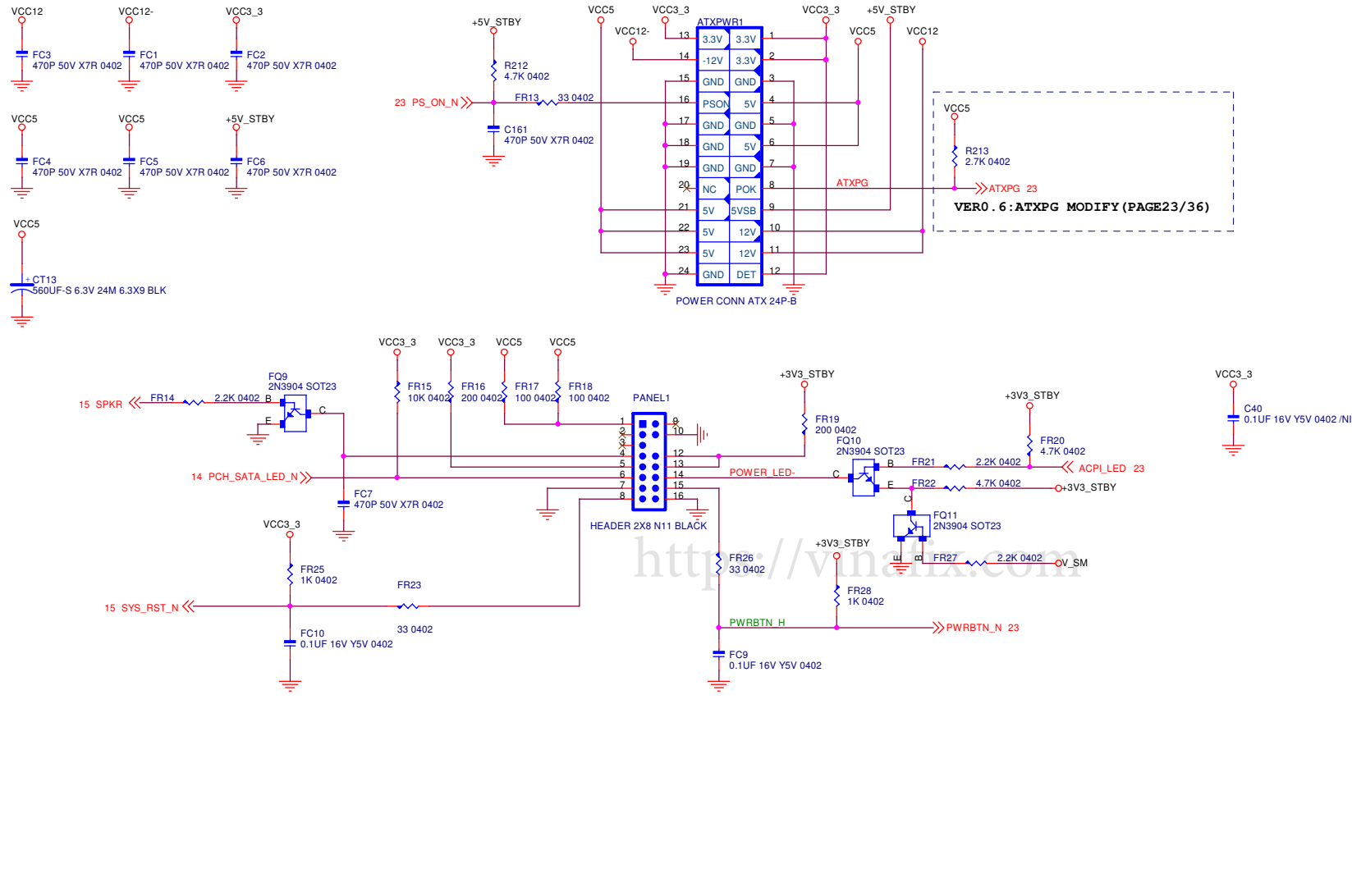
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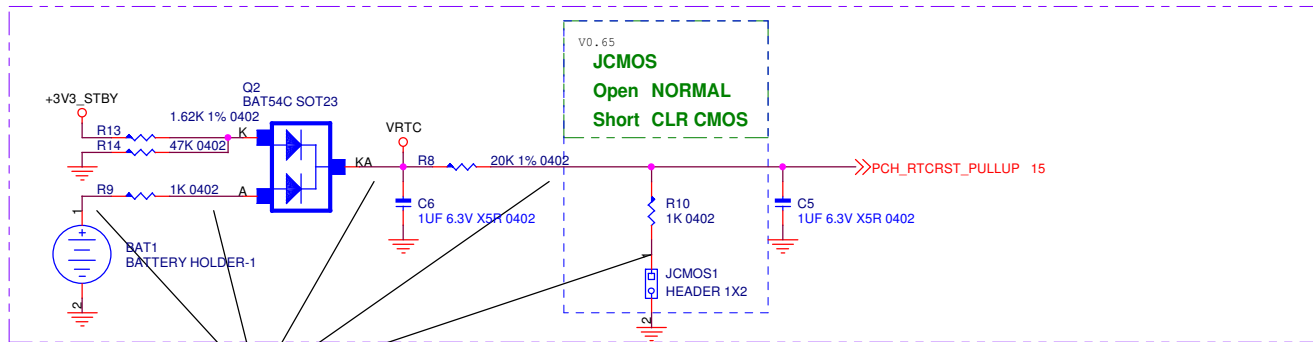
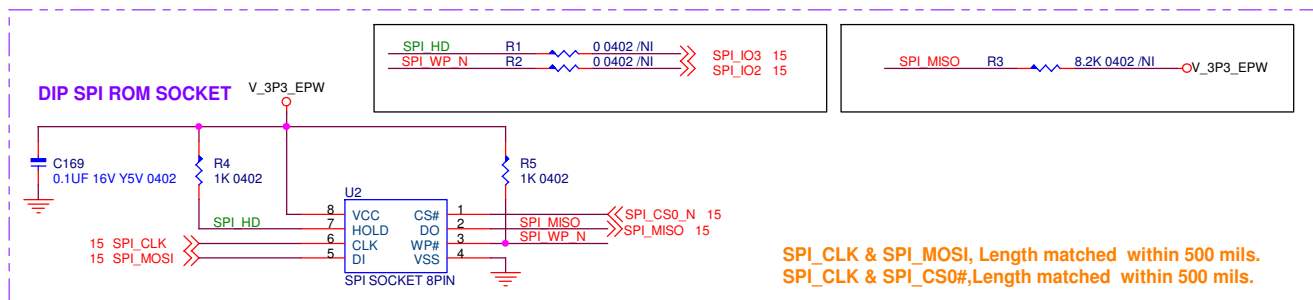
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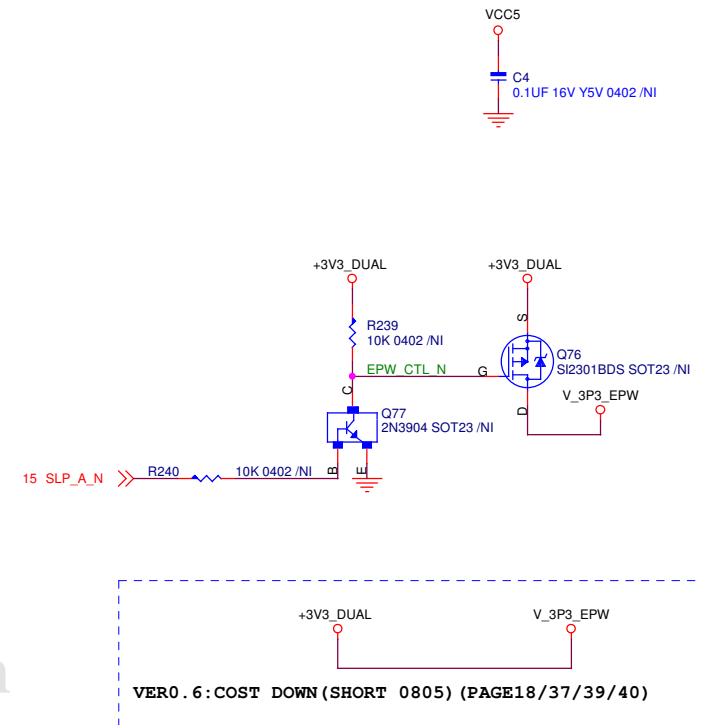

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Title 24PIN CONN & FP		
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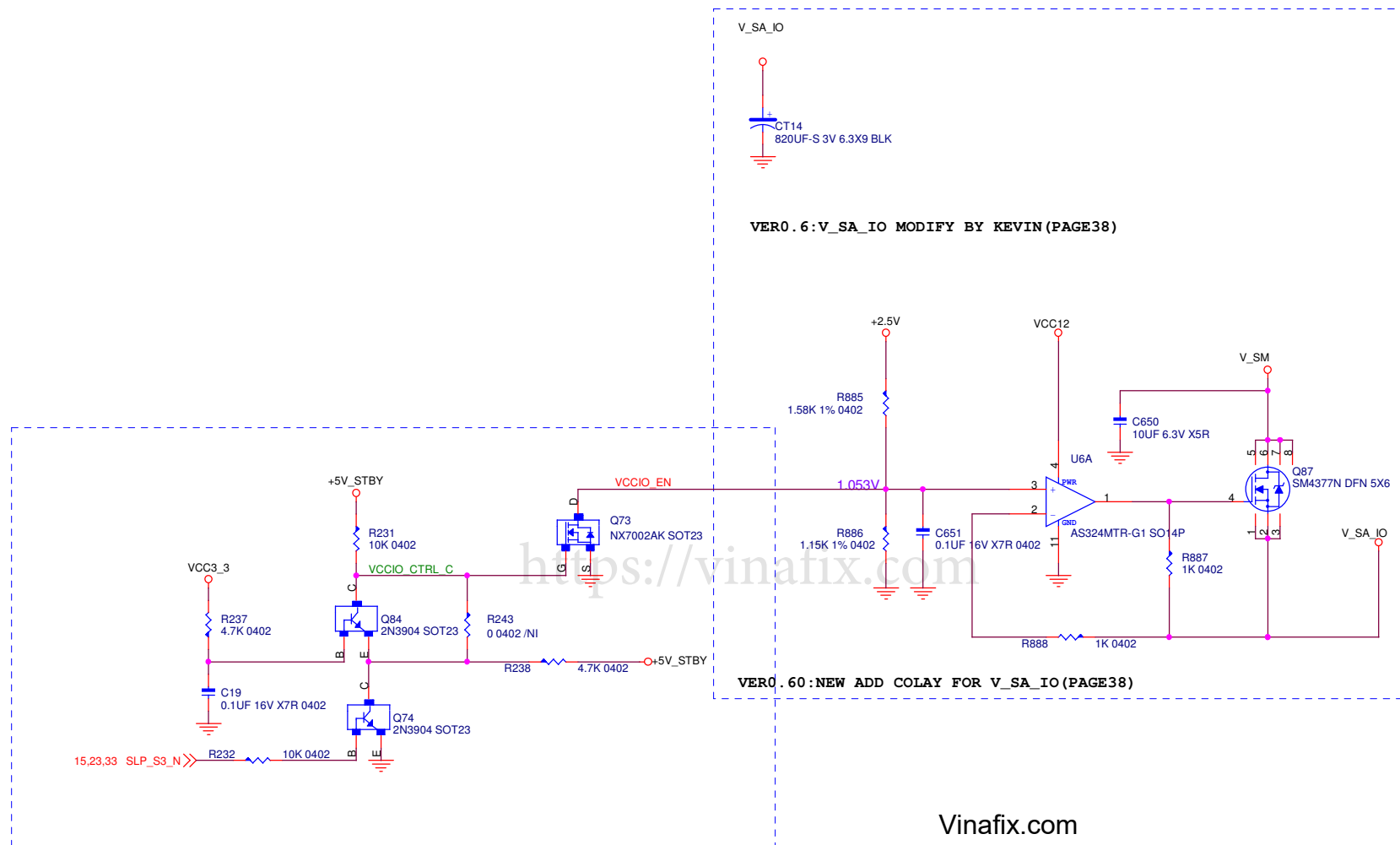
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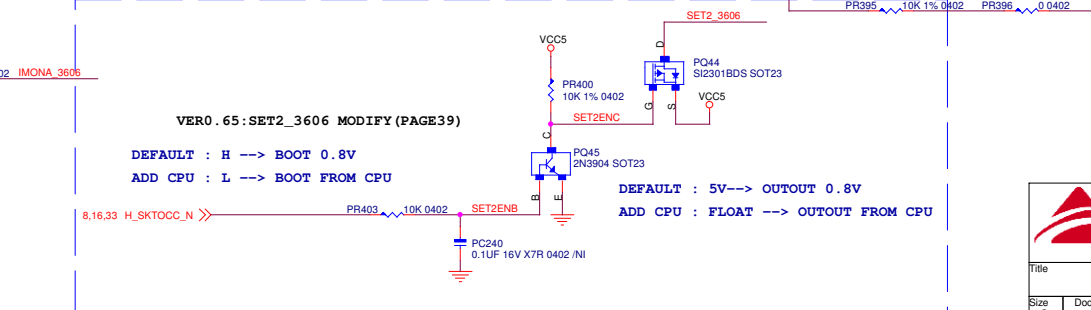
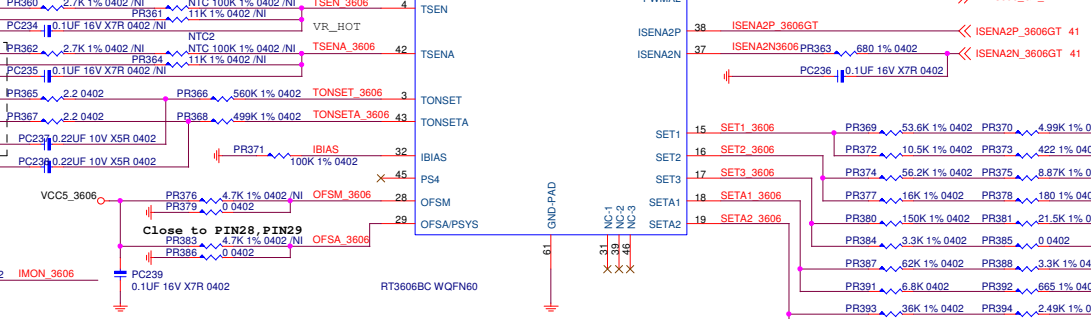
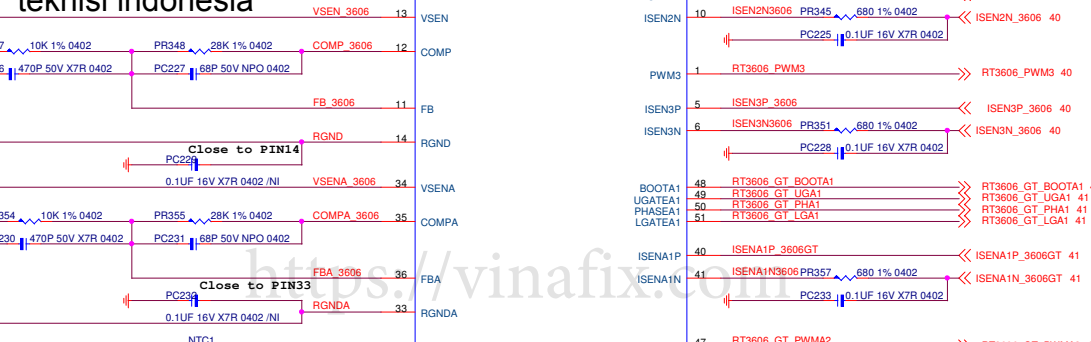
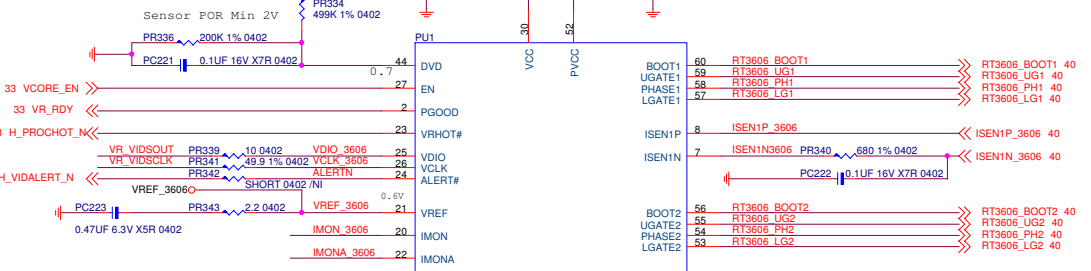
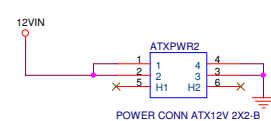
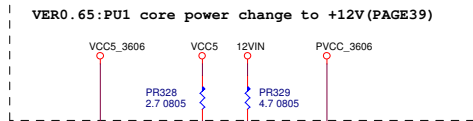
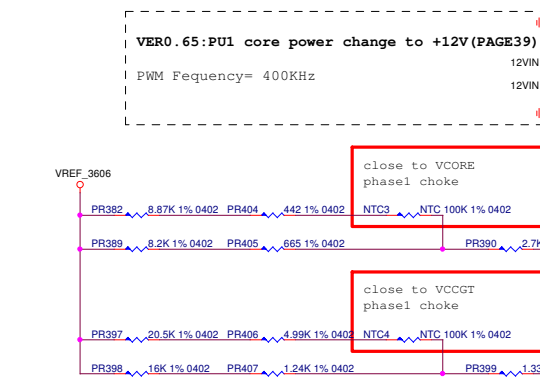
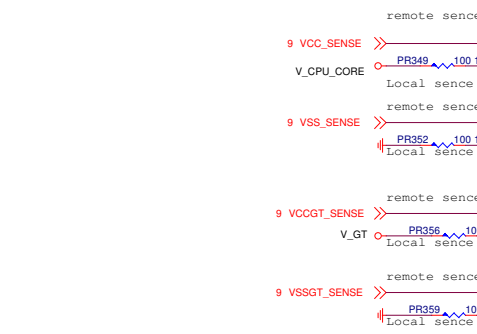
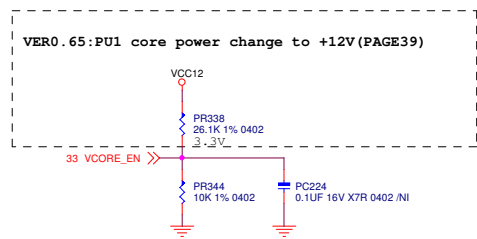


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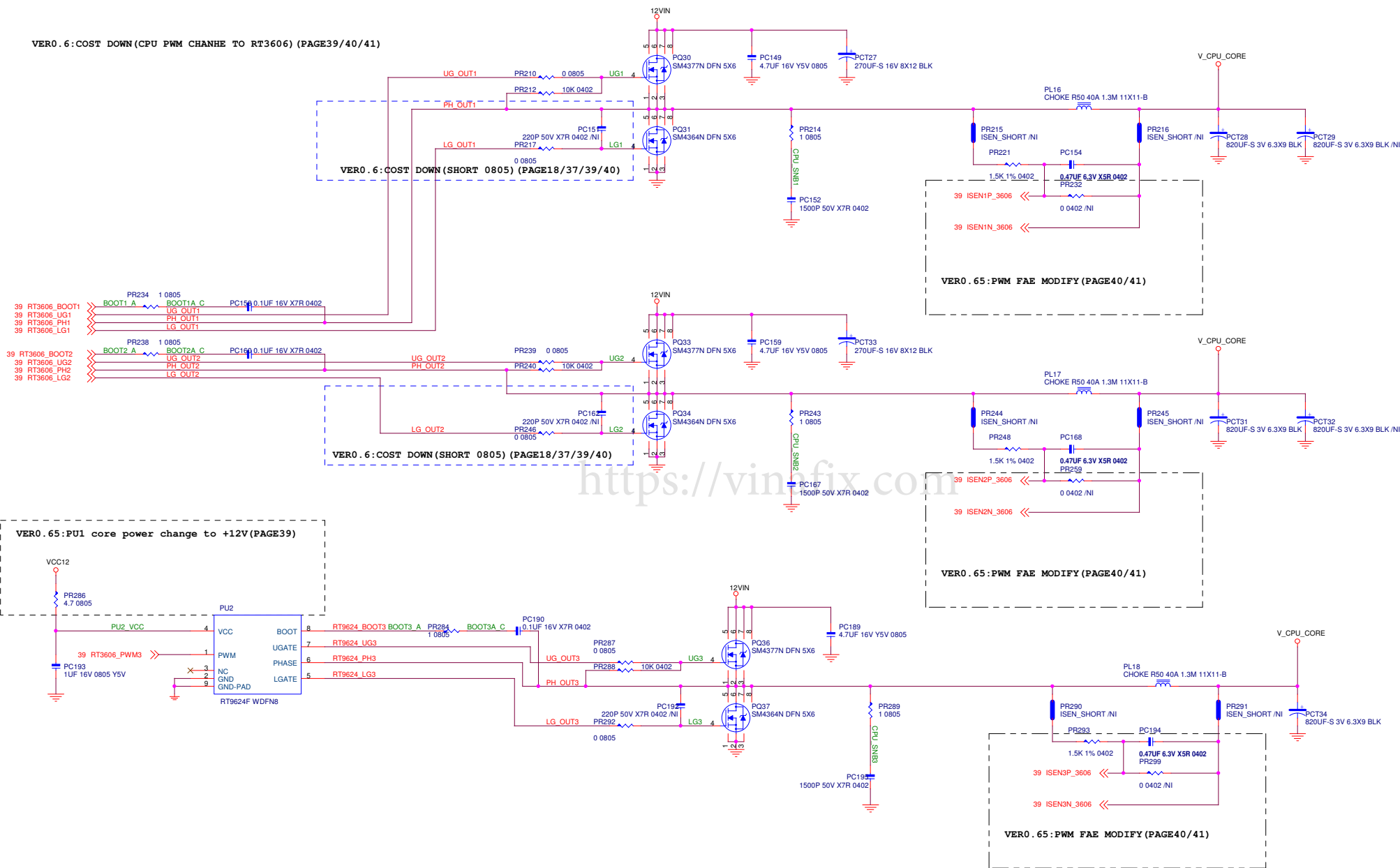
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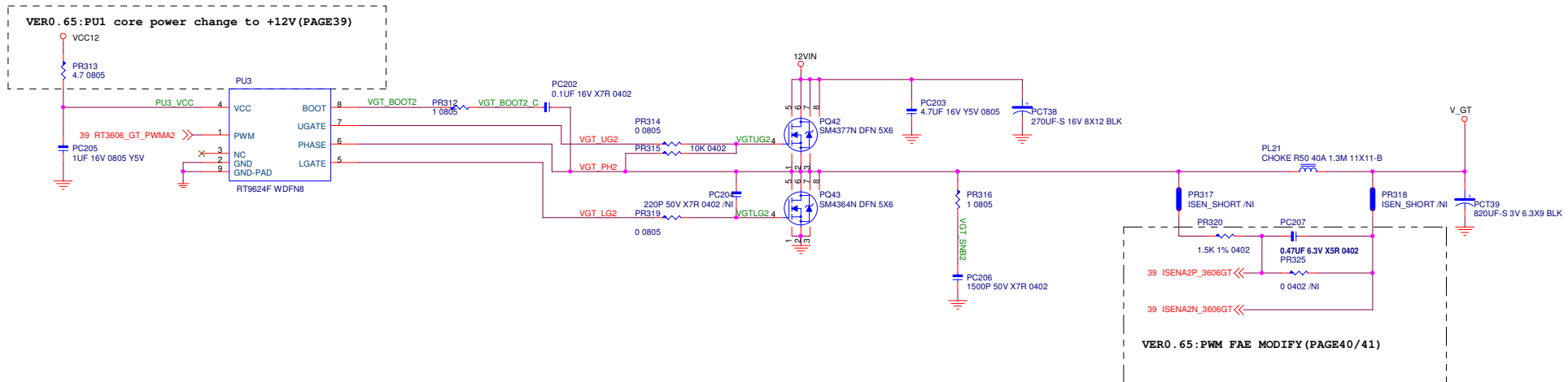
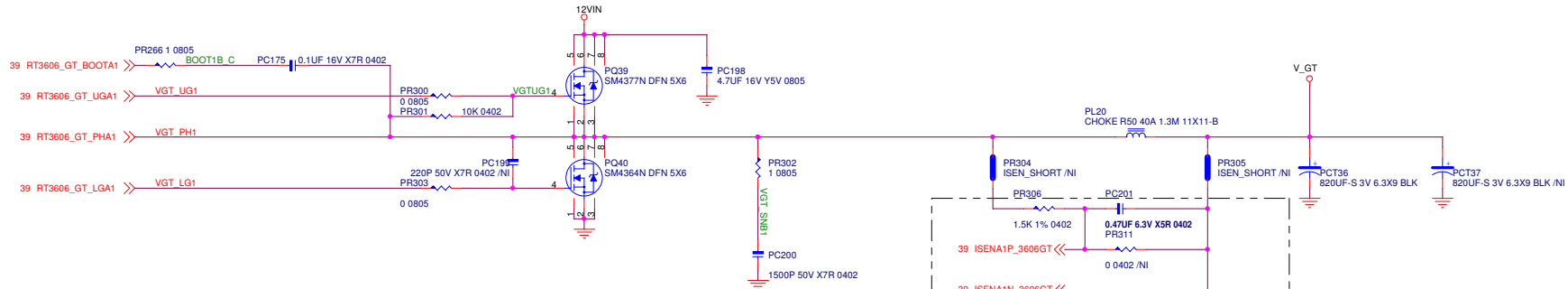
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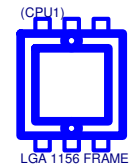
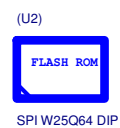
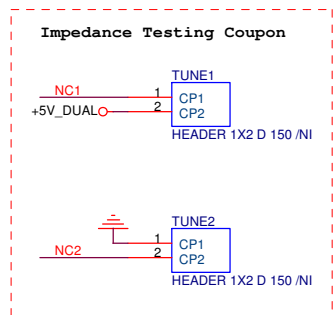
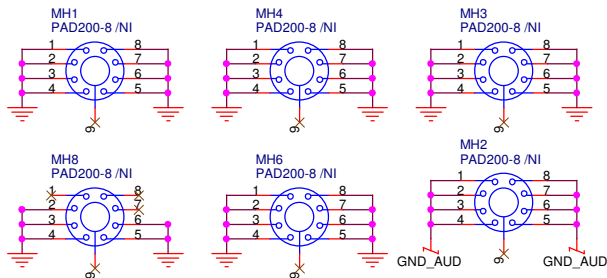



VER0.6:COST DOWN(CPU PWM CHANHE TO RT3606) (PAGE39/40/41)



Skylake S-line 42 95W RT3606_VGT







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